AN14116

Hardware Design Guidelines for S32M2xx Microcontrollers

Rev. 1 – October 2023 Application Note

1 Introduction

The S32M2XXC/L family is an automotive 32-bit microcontroller family using the NVM + UHV technology that offers the capability to integrate 40V analog components. This family reuses many features from the existing S32K1 and S32K3 portfolios. The particular differentiating features of the S32M2XX devices are the combination of MCU peripherals (ADC, FlexTimer, Communication interfaces, etc.), and the integration of “high-voltage” analog modules, including the voltage regulator (VREG), Gate Drive Unit (GDU), and either Local Interconnect Network (LIN) physical layer or CAN Physical layer. These features enable a fully integrated single-chip solution to drive up to 6 external power MOSFETs for BLDC, Switched Reluctance motor, or PMSM motor drive applications.

NOTE

Electrical parameters mentioned in this application note are subject to change in individual device specifications. Check each application against the latest data sheet for specific target devices.

2 Abbreviations, Acronyms and Definitions

The following list defines the abbreviations that might be used in this document.

BST	Boost
CCM	Counter with CBC MAC (Cipher block chaining message authentication code)
CMOS	Complementary Metal Oxide Semiconductor.
CP	Charge Pump
CPU	Central Processing Unit.
CSPI	Configurable Serial Peripheral Interface.
DDR	Double Data Rate.
DIP	Dual In-line Package.
DPGA	Differential Programmable Gain Amplifier
EEPROM	Electrically Erasable Programmable Read Only Memory.
EPROM	Erasable Programmable Read Only Memory.
FET	Field-Effect Transistor
GCTL	Gate Control
GDU	Gate Driver Unit
GPIO	General Purpose Input/output.
GPO	General Purpose Output.
HG	High-side Gate
HS	High-side Source
HW	Hardware.
HVI	High Voltage Input
HVM	High Voltage Module
I2C	Inter-Integrated Circuit.
I/O	Input/output.
JTAG	Joint Test Access Group.
LED	Light Emitting Diode.
LG	Low-side Gate
LPM	Low-Power Mode
LS	Low-side Source
MB	Megabyte.
MCU	Microcontroller Unit.
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MS	Memory Stick.
NVRAM	Non-volatile Random-Access Memory.
PCB	Printed Circuit Board.
PHY	Physical interface.
PMC	Power Management Controller
POR	Power-on Reset.
PSRAM	Pseudo Random Access Memory.
PWR	Power.
PWM	Pulse Width Modulation.
RAM	Random Access Memory.
SDRAM	Synchronous Dynamic Random-Access Memory.
TFT	Thin Film Transistor.
UART	Universal Asynchronous Receiver/Transmitter.
USB	Universal Serial Bus.

3 Power management

The power and ground pins are described in the Table 1 and the subsequent sections.

Table 1. *S32M2XX* – Power supply pins and domains

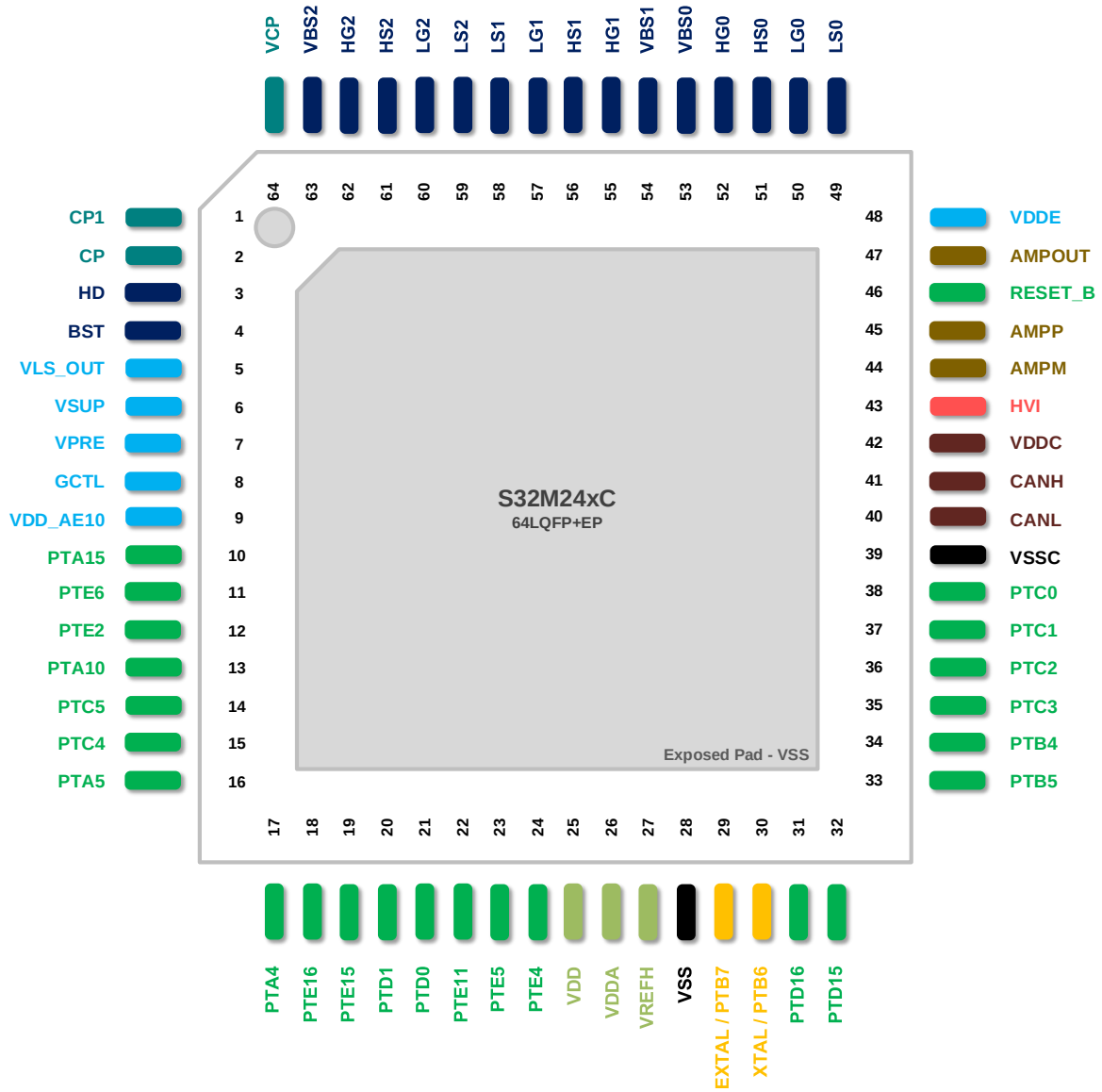
MCU Pin Name	Description	S32M24XC 64LQFP-EP	S32M24XL 64LQFP-EP	S32M27XC 64LQFP-EP	S32M27XL 64LQFP-EP	Notes
VSUP	Voltage regulator and LINPHY supply voltage.	6	6	6	6	
VDD_AE10	3.3V/5V application extension regulated for MCU supply.	9	9	9	9	For S32M2xx devices, VDD_HV_A, VDD[2], VDDA, and VDD_HV_A[1] must be connected to a common source plane (VDD_AE10) on PCB.
VDD[2]	MCU supply voltage.	25	25	-	-	
VDDA[2]	Analog supply voltage.	26	26	-	-	
VDD_HV_A[1]	Domain and Ref. voltage for I/O pins.	-	-	37	37	
		-	-	25	25	
		-	-	12	12	
VREFH	ADC high reference voltage.	27	27	23	23	
VDDC	CAN-FD PHY supply.	42	-	42	-	Internally generated.
VDDE	DC voltage on VDDE pin.	48	48	48	48	
V11[1]	Internal MCU Reference.	-	-	27	27	
		-	-	38	38	
V25[1]	Internal MCU Reference.	-	-	26	26	
BST	MOSFET pre-driver boost converter connection.	4	4	4	4	
VPRE	VPRE internally generated preregulation stage.	7	7	7	7	The VPRE voltage can be regulated using an external p-channel power FET (gate controlled via the GCTL pin).
HD	MOSFET pre-driver high-side drain voltage.	3	3	3	3	
VCP	MOSFET pre-driver charge pump output voltage.	64	64	64	64	
CP	MOSFET pre-driver charge pump driver output.	2	2	2	2	
CP1	MOSFET pre-driver charge pump charge & discharge node.	1	1	1	1	
VLS_OUT	MOSFET pre-driver supply, internally generated.	5	5	5	5	
VBS0	MOSFET pre-driver bootstrap capacitor connection.	53	53	53	53	
VBS1	MOSFET pre-driver bootstrap capacitor connection.	54	54	54	54	
VBS2	MOSFET pre-driver bootstrap capacitor connection.	63	63	63	63	
VSS	Supply Ground	28	28	28	28	
		65	65	65	65	
VSSC	Ground Pin for CAN Physical Layer.	39	-	39	-	
VSSL	Ground Pin for LIN Physical Layer.	-	41	-	41	

[1] Only available in the S32M27x devices.
[2] Only available in the S32M24x devices.

3.1 General view of the pinout and power domains for the S32M2 MCU family

This section shows an overview of the voltage domains for the different interfaces and I/Os in the MCU. Please refer to the latest version of the Datasheet and S32M2XX_IO_Signal_Description File for more details.

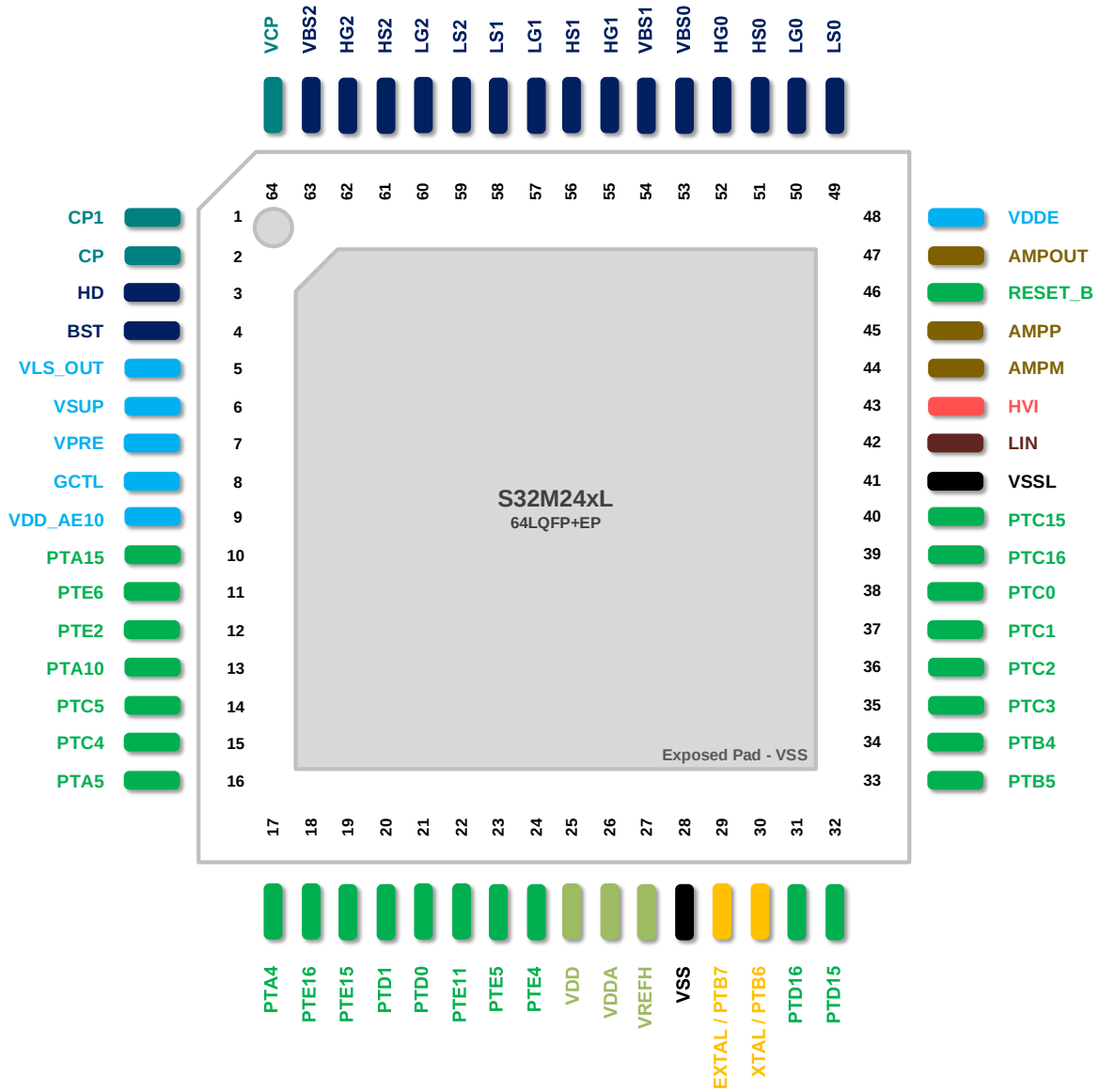
3.1.1 General view of the pinout and power domains for the S32M24xC - 64LQFP_EP Package



MCU Pin Function	#Pins
VDD, VDD_AE10, VDDA, and VREFH Power Pin	4
I/Os pins on the VDD Power Domain [including JTAG(4) and RESET(2)]	24
XTAL/EXTAL	2
PMC Pins	5
GDU Pins	17
Charge Pump Pins	3
DPGA Pins	3
HVI Pin	1
CAN PHY Pins	3
VSS and VSSC – Ground pins	2
TOTAL of pins	64

Figure 1. General view of the pinout and power domains for the S32M242C /44C - 64LQFP_EP Package

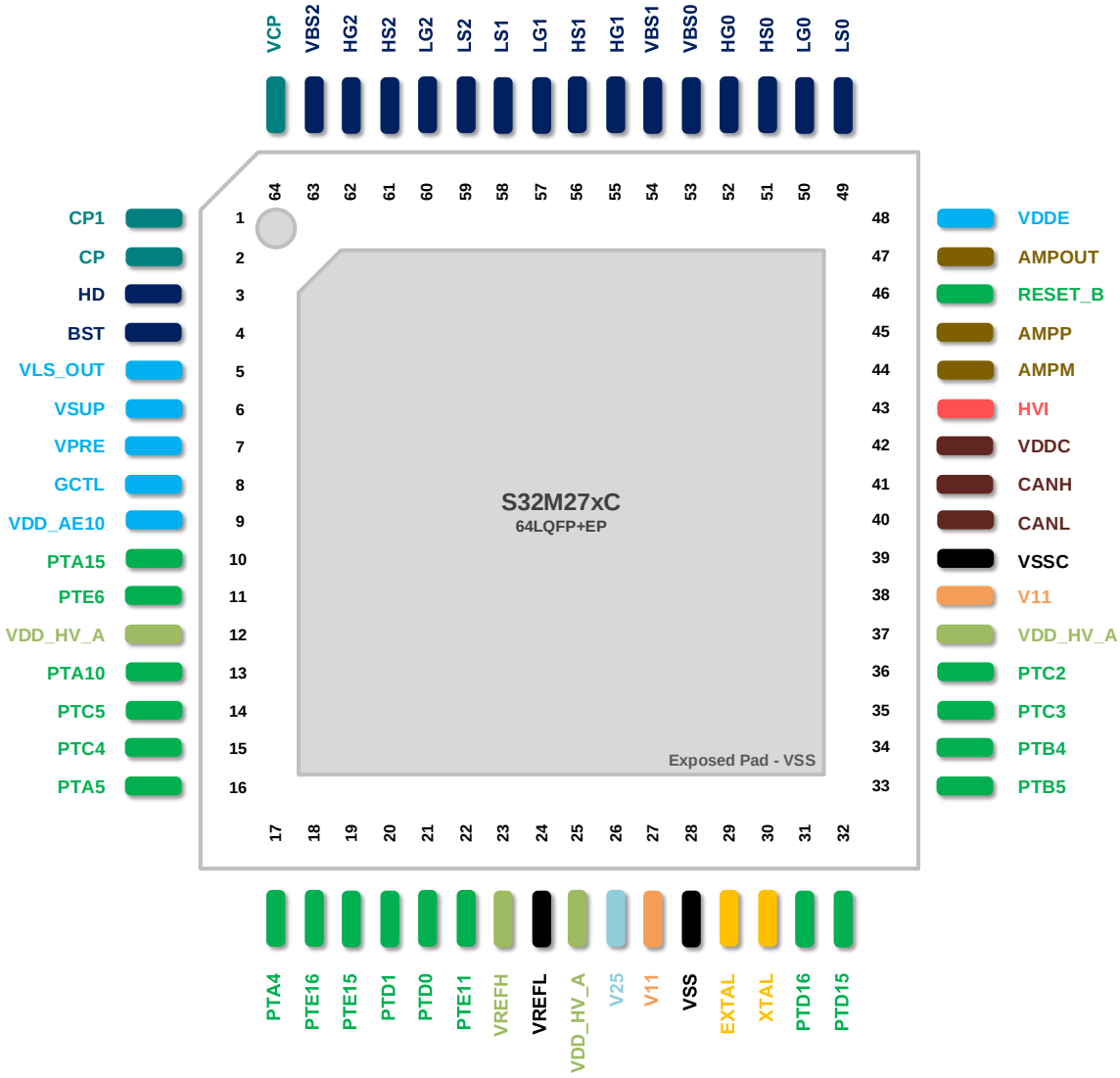
3.1.2 General view of the pinout and power domains for the S32M24xL - 64LQFP_EP Package



MCU Pin Function	#Pins
VDD, VDD_AE10, VDDA, and VREFH Power Pin	4
I/Os pins on the VDD Power Domain [including JTAG(4) and RESET(2)]	26
XTAL/EXTAL	2
PMC Pins	5
GDU Pins	17
Charge Pump Pins	3
DPGA Pins	3
HVI Pin	1
LIN PHY Pin	1
VSS and VSSL – Ground pins	2
TOTAL of pins	64

Figure 2. General view of the pinout and power domains for the S32M242L /44L - 64LQFP_EP Package

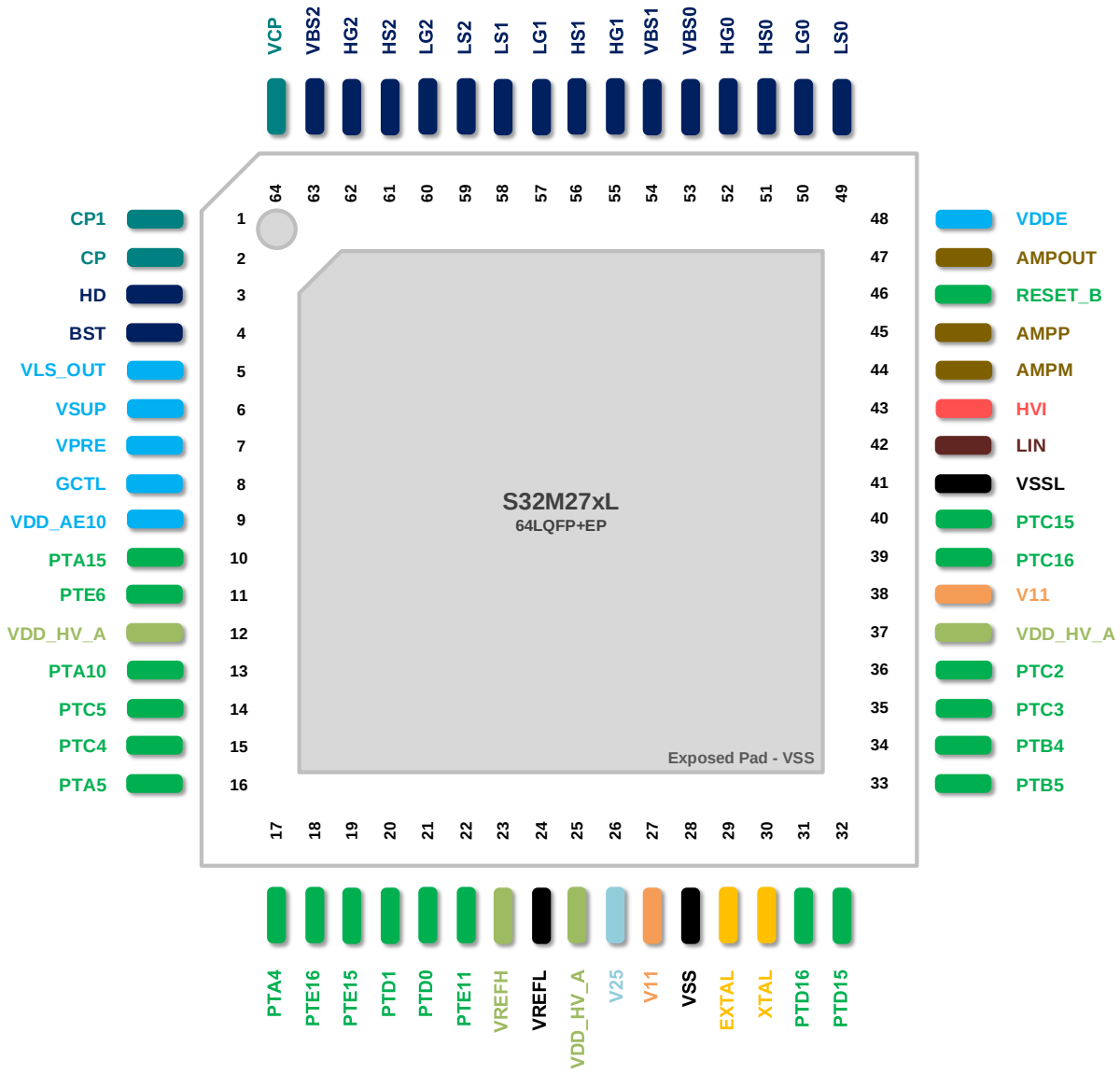
3.1.3 General view of the pinout and power domains for the S32M27xC - 64LQFP_EP Package



MCU Pin Function	#Pins
VDD_HV_A, VDD_AE10, and VREFH Power Pin	5
I/Os pins on the VDD_HV_A Power Domain [including JTAG(4) and RESET(2)]	19
V25 Power Pin	1
V11 Power Pins	2
XTAL/EXTAL	2
PMC Pins	5
GDU Pins	17
Charge Pump Pins	3
DPGA Pins	3
HVI Pin	1
CAN PHY Pins	3
VSS, VREFL, and VSSC – Ground pins	3
TOTAL of pins	64

Figure 3. General view of the pinout and power domains for the S32M276C - 64LQFP_EP Package

3.1.4 General view of the pinout and power domains for the S32M27xL - 64LQFP_EP Package



MCU Pin Function	#Pins
VDD_HV_A, VDD_AE10, and VREFH Power Pin	5
I/Os pins on the VDD_HV_A Power Domain [including JTAG(4) and RESET(2)]	21
V25 Power Pin	1
V11 Power Pins	2
XTAL/EXTAL	2
PMC Pins	5
GDU Pins	17
Charge Pump Pins	3
DPGA Pins	3
HVI Pin	1
LIN PHY Pin	1
VSS, VREFL and VSSL – Ground pins	3
TOTAL of pins	64

Figure 4. General view of the pinout and power domains for the S32M276L - 64LQFP_EP Package

3.2 VSUP — Input power supply pin

VSUP is the input supply voltage pin for the on-chip voltage regulator. An input supply voltage is used for the generation of on-chip supply voltages. VSUP pin must be protected by external components, i.e., a diode against a reverse battery connection, as seen in Figure 5 with an external diode or in **Figure 6** with a boost converter, which contains a diode protecting VSUP pin.

The designer could choose to add bulk with a bypass capacitors as a charge tank to mitigate a fast decrease of input voltage when losing battery. The value of this capacitor depends on the current consumption of the system and the time interval needed for the MCU to perform housekeeping activities before shutting down.

The LIN/HV Physical Layer can be supplied by either a VSUP pin or an HD pin.

3.3 VPRE — Voltage Pre-Regulator

The device supports the use of an external p-channel power FET to supplement the VDD supply for reducing on-chip power dissipation. In this configuration, most of the current flowing from VBAT to VDD flows through the external power FET. This configuration is controlled via the GCTL pin.

3.4 GCTLC — Gate control pin for p-channel power FET

GCTL connects to the gate of an external power FET, which is used to regulate the VPRE from the VSUP. This is an excellent option to reduce heat and power consumtion in the S32M2 MCU.

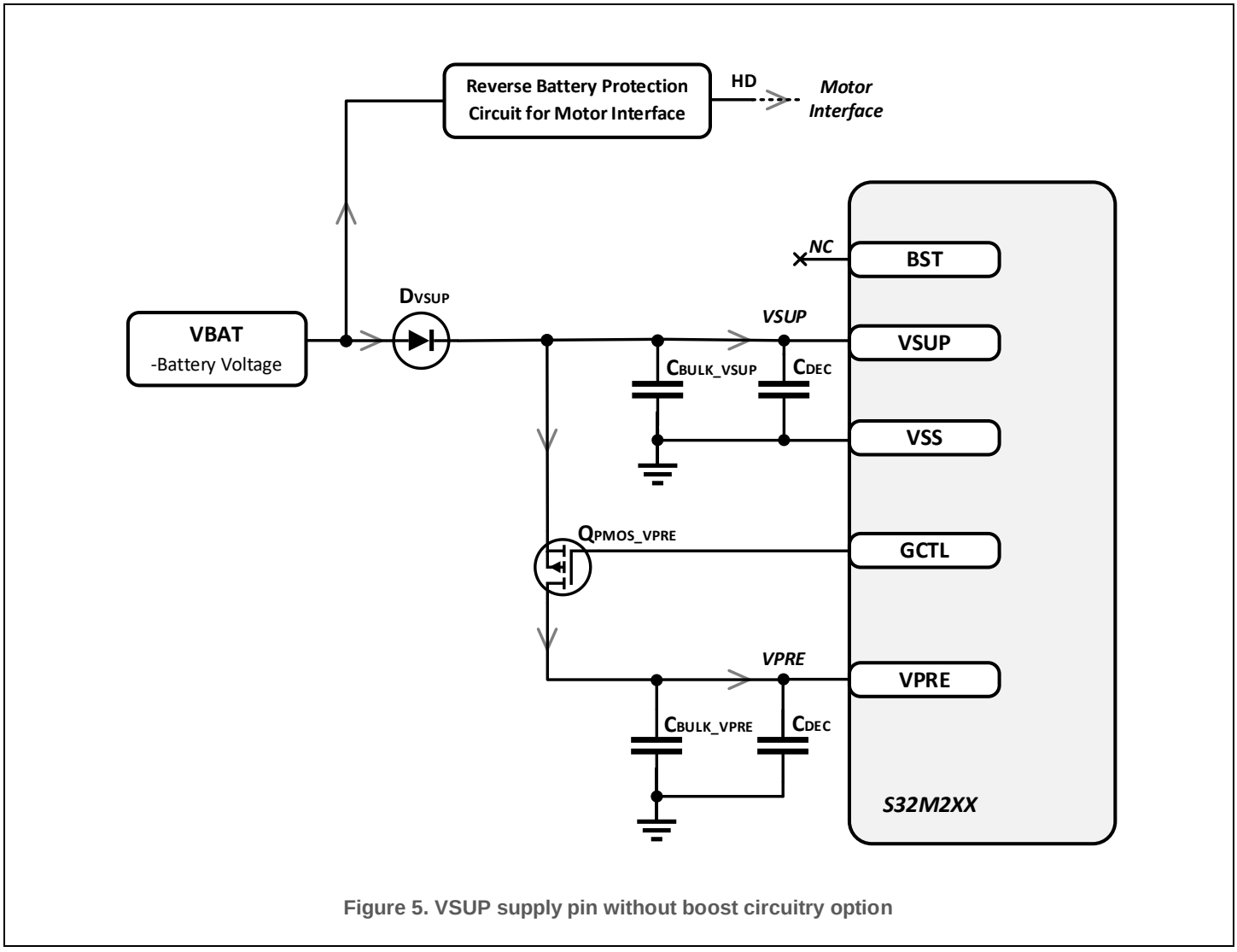


Figure 5. VSUP supply pin without boost circuitry option

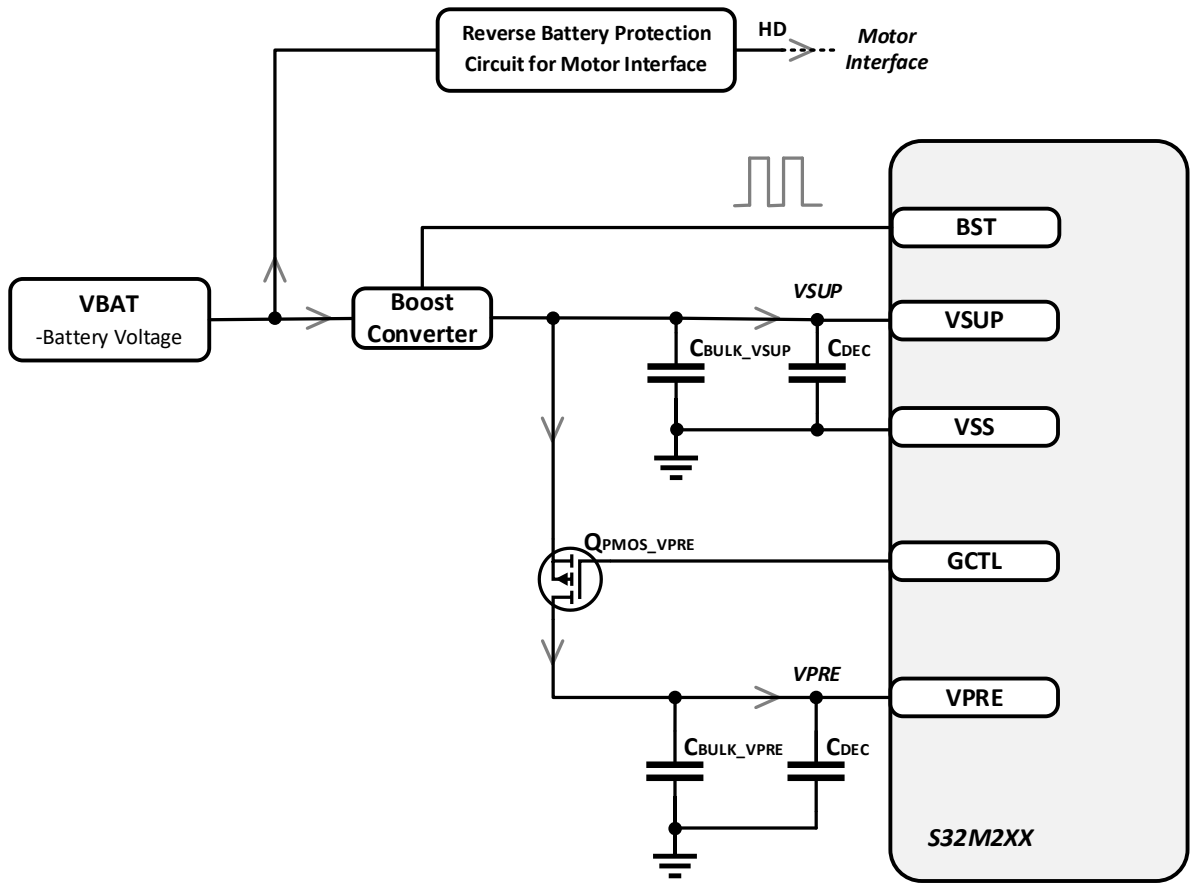


Figure 6. VSUP supply pin with BOOST converter

Table 2. Components description and values

Symbol	Characteristic	Value
D_{VSUP}	Reverse battery protection diode dedicated for VSUP.	
Q_{PMOS_VPRE}	P-Channel power MOSFET.	
C_{BULK_VSUP}	Bulk/Bypass capacitor.	2.2uF – 4.7uF[1]
C_{BULK_VPRE}		
C_{DEC}	Decoupling capacitor.	100nF - 220nF[1]

1. Datasheet information.

Make sure to put the decoupling capacitor as close as possible to the MCU. Shortening the capacitor traces to/from the ground/power plane is the most important concern for making a low-inductance connection. In order to implement an appropriate decoupling for applications with LIN, CAN, SPI, and I2C interfaces, consider the pairing of the power and ground planes close to each other (less than 10 mils). This creates an effect of interplane capacitance, greatly reduces noise, and increases power supply stability at the pins because of the extremely low inductance of this kind of capacitance in the layers. The number of discrete capacitance can be reduced because the practical capacitors are significantly increased, and the power distribution network impedance is reduced across a very broad frequency range.
The number of discrete capacitance can be reduced because the effective capacitors are greatly increased, and the impedance of the power distribution network is reduced across a very broad frequency range.

3.5 VDD_AE10 and VDD — Digital I/O and Logic Supply

The VDD belongs to the MCU die and supplies core, memory, and digital systems inside of the microcontroller. It can be configured to be either 3.3V or 5V. It is internally generated from VPRE. VDD pin exists only in S32M24x devices, as shown in Figure 7 and Figure 8. The VDD_AE10 belongs to the analog die side and provides energy to the microcontroller over the VDD pin. An external bulk capacitor in the range of 2.2uF to 4.7uF is required. VDD_AE10, VDD, and VDDA must be connected together to a common reference plane on PCB, as shown in Figure 9 and Figure 10.

3.6 VDDA — Analog Supply pins

The analog modules of MCU, i.g. AD converter are powered via the VDDA of S32M24x. In S32M27x devices, VDDA pin is not availbale. Generally, VDDA is connected together with VDD and the VDD_AE10 in a common source plane on PCB. Appropriate decoupling capacitors is needed in order to filter noise on the supplies. If higher noise is generated by VDD pin, then designer can use external stable voltage source for VDDA.

3.7 VREFH — Analog Reference Supply pin

The VREFH represents an input pin of the ADC reference voltage. VREFH should always supply by voltage, which is equal to or less than the supply rail + 0.1 V (VDDA + 0.1V and VDD + 0.1 V, or VDD_HV_A + 0.1V). If this pin is connected to another supply another CDEC is requiered near of the VREFH pin.

3.8 VDDC — CAN supply pin

VDDC is generated by internal voltage regulator from VPRE, typical 5V, and the internal regulator can be enabled or disabled. If it is enabled, VDDC is automatically turned off in LPM and after wake-up from LPM, VDDC is automatically turned on again. An external bulk capacitor in the range of 2.2uF to 4.7uF is required. This voltage reference should not be taken to power any other peripheral.

3.9 VDDE — Configurable pin

VDDE is a configurable source which can be used in two modes: digital mode, and analog mode. When used in analog mode, the VDDE pin can drive a strong VDD voltage or a weak GND. In the digital mode, can be set for CANPHY_TX, LINPHY_TX, or not used and not driven. However, for mode selecting, refer to reference manual".

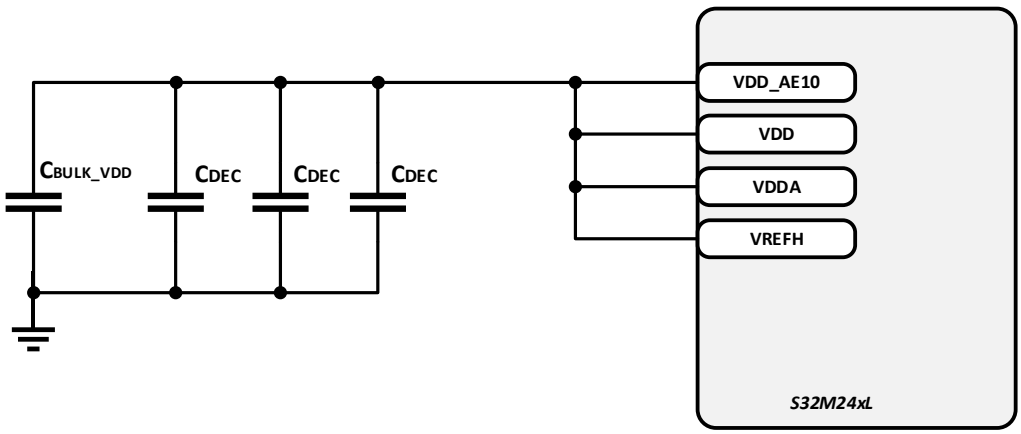


Figure 7. Logic supply's for S32M24XL

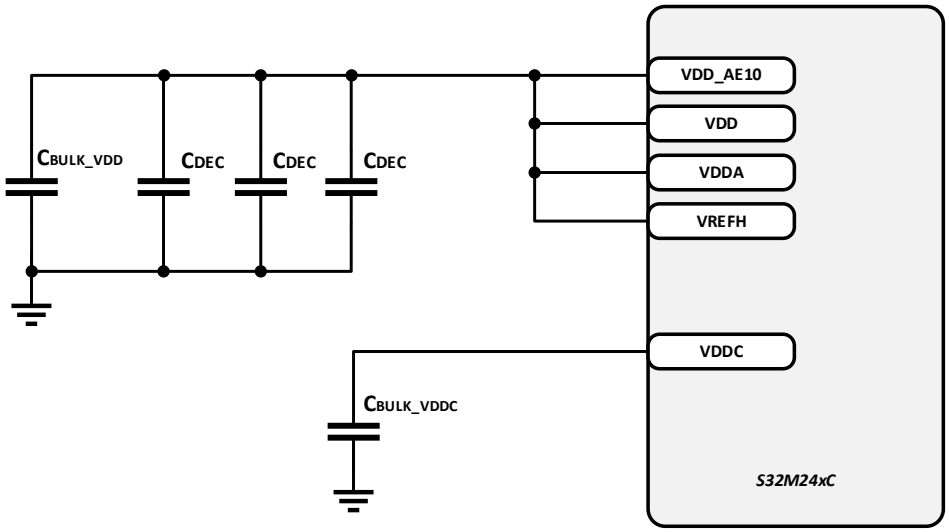


Figure 8. Logic supply's for S32M24XC

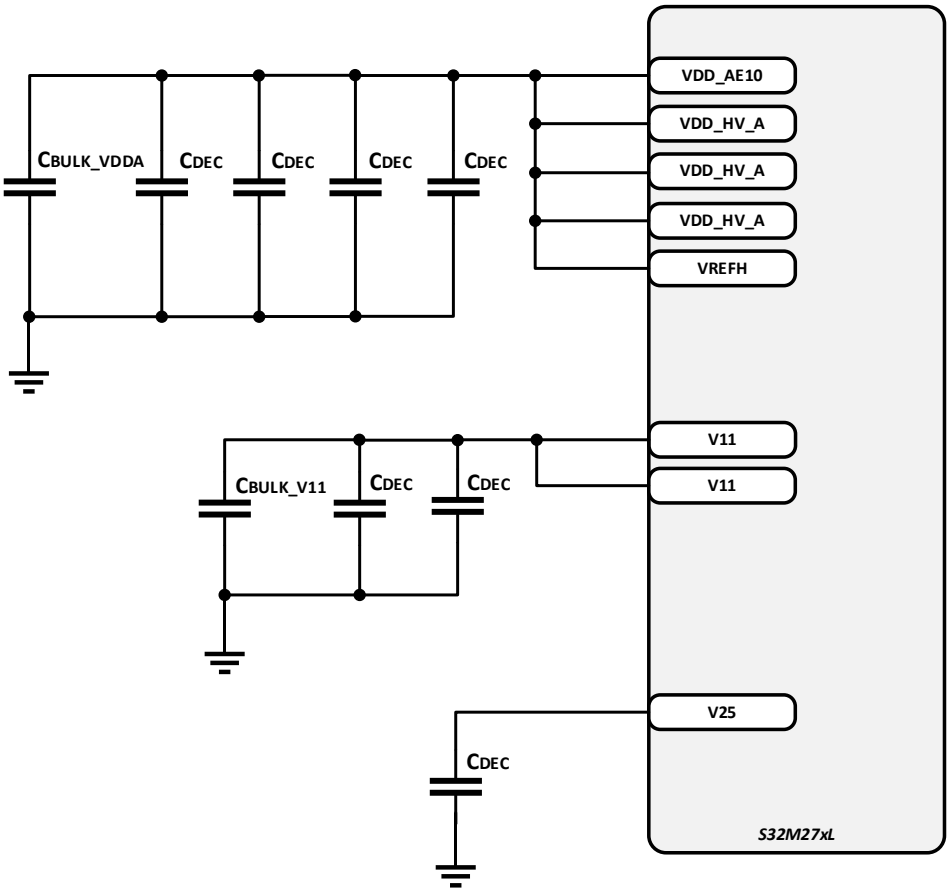


Figure 9. Logic supply's for S32M27XL

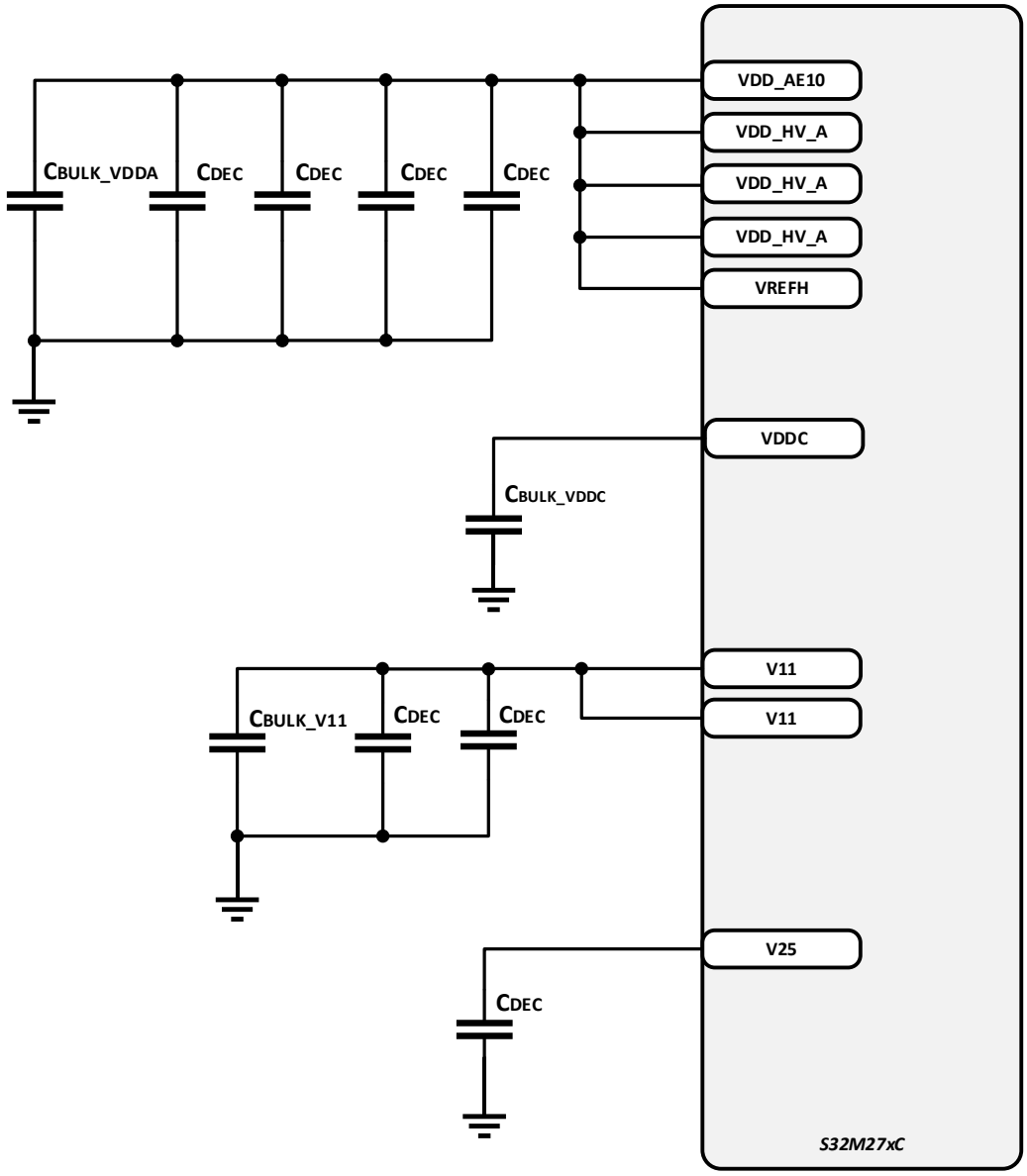


Figure 10. Logic supply's for S32M27XC

Table 3. VDD - component description and recommended value

Symbol	Characteristic	Value
C_{BULK_VDD}	X7R / X8R Ceramic	2.2 uF – 4.7uF
C_{BULK_VDDC}		
C_{BULK_VDDA}		
C_{BULK_V11}		
C_{DEC}	X7R / X8R Ceramic	100nf - 220nF

3.10 Selecting the external p-channel power FET

The maximum VREG current capability using an external p-channel power FET must be determined by the allowed maximum power of the device. The designer should consider that the maximum power dissipation of the transistor will depend mainly on the following factors:

- Package type
- Dissipation mounting pad area on the PCB
- Ambient temperature

Drain-source voltage and maximum junction temperature of power MOSFET are key parameters that mustn't be exceeded. This is a critical point since the lifetime of all semiconductors is inversely related to their operating junction temperature. For almost all transistor packages, the maximum power dissipation is specified at +25°C; above this temperature, the power derates to the maximum junction temperature (+150°C). The parameter RthJA(thermal impedance between junction to ambient) depends mostly on the package of the transistor and the mounting pad area as shown in the Figure 11. The final product's thermal limits should be tested and qualified to ensure acceptable performance and reliability.

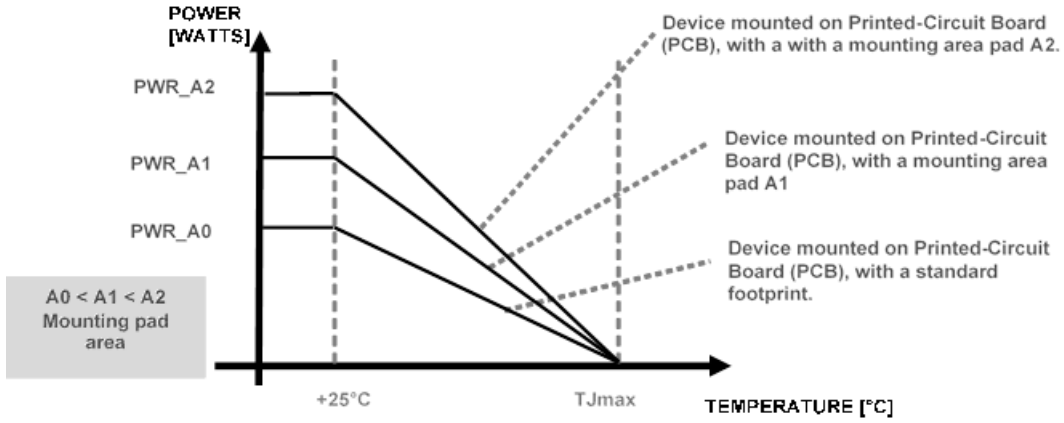


Figure 11. Maximum power dissipation versus temperature

The maximum power dissipation PWR_{MAX} by the device is given by:

$$PWR_{MAX} = \frac{T_{JMAX} - T_{ambMAX}}{R_{thJA}}$$

Equation 1.

where T_{ambMAX} is ambient temperature, T_{jMAX} is maximum junction temperature and R_{thJA} is the Junction to Ambient Thermal Resistance of the power FET mounted on the specific PCB.

3.10.1 Recommended P-channel power FET

Table 4. *S32M24x* - Recommended power transistor

Part Number	Package Type	Manufacturer
BUK6Y61-60PX (Actually used in the EVB)	LFPAK56	NEXPERIA
SQS401EN-T1-BE3	PowerPAK 1212-8W	VISHAY
BUK7M8R5-40HX	LFPAK-33-8	NEXPERIA

The designer must follow and verify all layout/soldering footprint recommendations of the transistor supplier to reach a good performance of MOSFET. Make sure to put the decoupling capacitor as close as possible to the MOSFET.

3.11 VSSX, VREFL, and VSSC – MCU Ground Reference

All VSSx, VREFL, and VSSC pins of the MCU must be externally connected together in a continuous and single solid GND plane.

Table 5. *S32M2xx* – MCU Ground reference

MCU Pin Name	Description	S32M2xx MCU Package - Pin Number				Notes
		S32M24xL 64LQFP + EP	S32M24xC 64LQFP + EP	S32M27xL 64LQFP + EP	S32M27xC 64LQFP + EP	
VSSx		28	28	28	28	All MCU's VSSx VREFL and VSSC pins must be externally connected in a continuous and single solid GND plane on the PCB.
		65	65	65	65	
VSSC	Ground Pin for CAN Physical Layer The VSSC pin is the return path for the 5V supply (VDDC).	-	39	-	39	
VSSL		41	-	41	-	
VREFL		-	-	24	24	
EP	Exposed pad	65	65	65	65	

4 High Voltage Inputs (HVI)

This chip implements a high voltage module (HVM) with 2 high voltage inputs (HVI) and one voltage monitor (VM). HVI0 is connected to the device VSUP pin. HVI1 is connected to the HVI pin. The VM is dedicated to HVI0 for battery voltage monitoring.

The high-voltage input (HVI) has the following features:

- A voltage divider to divide down different input voltage levels to the system voltage.
- Event generation, when the input logic level changes. This works also when the clock is off, so you can use this digital input interrupt, for example, to wake up the device from sleep mode.
- Event observation through interrupt generation, reading of an interrupt flag in a register or polling the event status from a register.
- Analog output, for example, reading the input voltage with an on-chip ADC.
- Selectable pull-up and pull-down connections on the input for open input detection.
- Voltage range limited to -0.3V < VHVI < 42V.

Note that the following procedures use a function that overrides the automatically disable mechanism of the digital input buffer when using the HVI in analog mode. Make sure to switch off the override function when using the HVI in analog mode after completing the check. An external 10 kΩ resistor R_{EXT_HVI} must be connected to the high-voltage inputs to protect the device pins from fast transients and to achieve the specified pin input divider ratios when using the HVI in analog mode as shown in the Figure 12. Internally this pin integrates a voltage divider to divide down the signal on the high voltage input by a configurable division. In order to obtain more information to configure this consult the High Voltage Module chapter in the reference manual that HVI input pin.

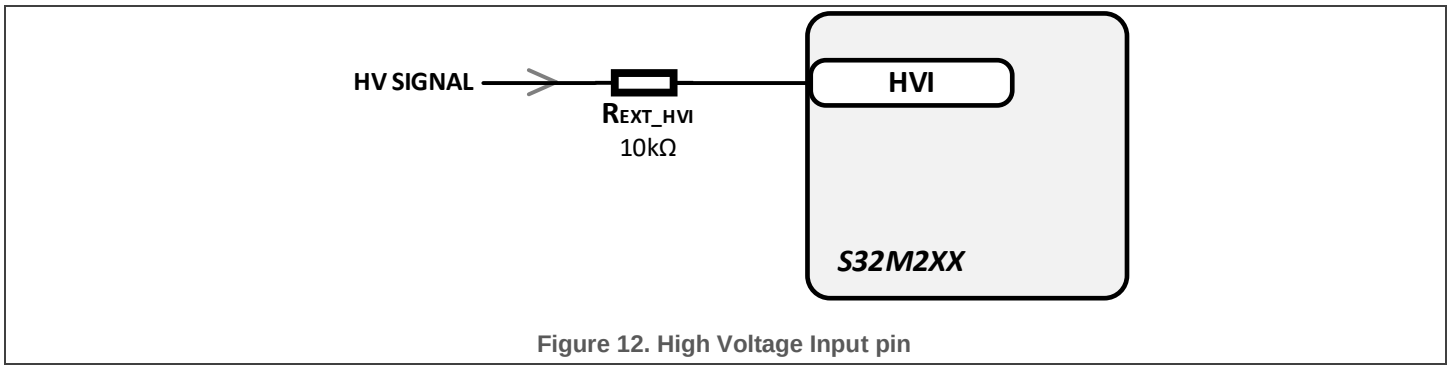


Figure 12. High Voltage Input pin

5 Debug and programming interface

5.1 RESET system

Resetting the MCU provides a way to start processing from a known set of initial conditions. System reset begins with the on-chip regulator in full regulation and system clocking generation from an internal reference.

5.1.1 External pins RESET

For all reset sources, the RESET pins are driven low by the MCU for at least 128 bus clock cycles until flash memory initialization has been completed. Once flash memory initialization has been completed, the RESET pins are released, and the internal chip reset de-asserts. Keeping the RESET pins asserted externally delays the negation of the internal chip reset. The RESET pins are the same as the standard GPIO. It can operate as a pseudo-open-drain output because there is also a PMOS device in the output stage.

The reset pins, similar to some other GPIO has a weak internal pull-up. If the environment and the customer application are noisy, an external pull-up resistor to VDD must be added directly to the reset pin in order to avoid a sporadic or unintended reset event. Refer to the device datasheet for the levels of voltage and current allowed in the pin. A capacitor in the reset line is not directly required for the MCU. In some cases, in order to add further ESD protection, an external capacitor is added between the RESET pin and the ground, and this capacitor must be placed as close as possible and directly to the debug interface or connector. The values of the pull-up resistor and the capacitor must be selected according to the design requirements of the application. Refer to the device datasheet for the minimum RESET pulse value that can be detected for the MCU.

Both of the reset pins (PTA5 and RESET_b) must always be shorted together externally to a common reference on PCB.

5.2 JTAG and SWD interface

A number of commonly used debug pins are shown here. Most of the Arm® development tools use one of these pins. At the moment when the circuit board is in development process, it is recommended to use a standard debug signal arrangement to make a connection to the debugger easier.

Table 6. JTAG signal description

Signal Name	Signal Description	MCU Pin Name	S32M2xx MCU Package - Pin Number				Recommendation[2]	I/O Power Domain
			S32M24xC 64LQFP + EP	S32M24xL 64LQFP + EP	S32M27xC 64LQFP + EP	S32M27xL 64LQFP + EP		
JTAG_TDO	JTAG Test Data Output	PTA10	13	13	13	13	Pull-Up	VDD
JTAG_TDI	JTAG Test Data Input	PTC5	14	14	14	14	Pull-Up	
JTAG_TCK/ SWD_CLK	Clock into the core	PTC4	15	15	15	15	Pull-Down	
JTAG_TMS/ SWD_DIO	JTAG Test Mode Select	PTA4	17	17	17	17	Pull-Up	
RESET[1]	Reset MCU[1]	PTA5	16	16	16	16	Pull-Up	
		RESET_B	46	46	46	46		

1. Reset pins must always be shorted together externally to a common reference on PCB. Refer to the RESET system and Debug and programming interface.
2. External pull-up/down resistors for the JTAG signals can be added to increase debugger connection robustness.

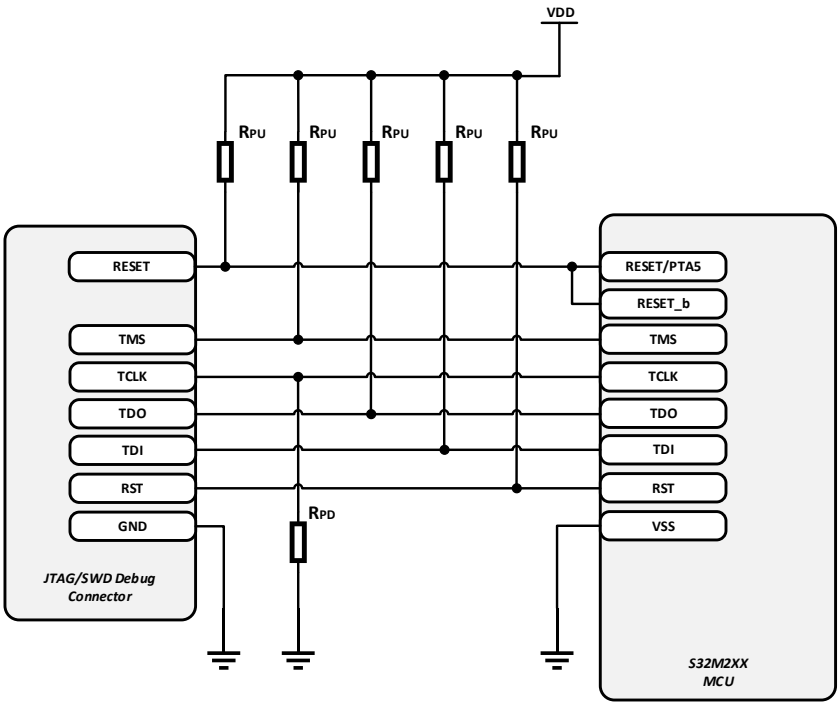


Figure 13. JTAG Pin Connections

Table 7. JTAG connector – Component description

Symbol	Parameter	Typ Value Range	Units
R_{PU}	Pull up Resistor	4.7k-10k	Ω
R_{PD}	Pull down Resistor	4.7k-10k	Ω

5.3 Debug connector pinouts

5.3.1 10-pin Cortex® Debug connector

For devices without ETM, you can use an even smaller 0.05” 10-pin connector (*Samtec FTSH-105)* for debugging. Similar to the 20pin Cortex® Debug D ETM connector, both JTAG and Serial-Wire debug protocols are supported in the 10-pin version.

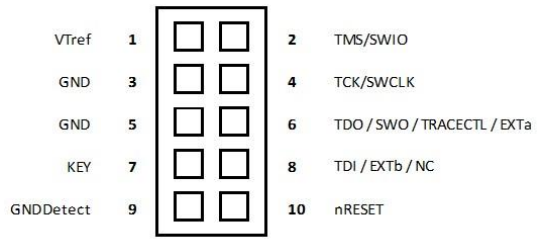


Figure 14. 10-pin Cortex® Debug connector pin layout

6 Clock circuitry

The S32M2XX MCU has the following clock sources

- FIRC (Fast Internal RC) Oscilator 48 MHz
- SIRC (Slow Internal RC) Oscilator 32 kHz
- PLL (Phase Locked Loop) up to 640 - 1280 MHz
- FXOSC (Fast External) Oscilator 8 - 40 MHz

Nevertheless the only clock source that must be considered from hardware design perspective is the FXOSC. This external oscillator works with a range from 8 to 40 MHz and that output can be used as a clock source for some peripherals or used with the PLL interface.

6.1 EXTAL and XTAL

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. The pierce oscillator provides a robust, low-noise, low-power external clock source. It is designed for optimal start-up margins with typical crystal oscillators. S32M2XX supports crystals or resonators from 8 MHz to 40 MHz The Input Capacitance of the EXTAL and XTAL pins is 7 pF.

Table 8. EXTAL and XTAL pins

MCU Pin Name	Description	S32M24XL	S32M24XC	S32M27XL	S32M27XC	Notes
		64 LQFP-EP	64 LQFP-EP	64 LQFP-EP	64 LQFP-EP	
XTAL	External Crystal Output	30	30	30	30	
EXTAL	External Crystal Input	29	29	29	29	

On reset, all the device clocks are derived from the internal PLLCLK, independent of EXTAL and XTAL. Where XTAL is the oscillator output.

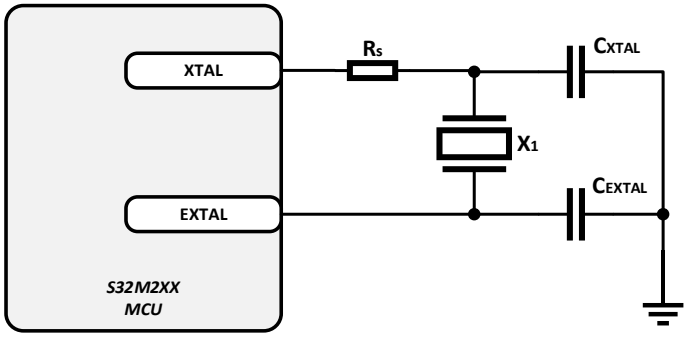


Figure 15. Reference oscillator circuit

Table 9. Oscillator circuit components description

Symbol	Description
Rs^1	Series resistor for current limitation
X_1	Quartz Crystal / Ceramic Resonator
C_{XTAL}	External load capacitor on XTAL pin.
C_{EXTAL}	External load capacitor on EXTAL pin.

1. The R_S and load capacitors values are dependent on the specifications of the crystal and on the board capacitance. It is recommended the customer develops an evaluation and characterization of the crystal on their PCB with the part manufacturer.

6.1.1 Suggestions for the PCB layout of the oscillator circuit

The crystal oscillator is an analog circuit and must be designed carefully and according to the analog-board layout rules:

- It is recommended to send the PCB to the crystal manufacturer to determine the negative oscillation margin as well as the optimum regarding R_S, $C_{XTAL}$and C_{EXTAL}capacitors. The datasheet includes recommendations for the tank capacitors $C_{XTAL}$and C_{EXTAL}. These values together with the expected PCB, pin, etc. stray capacity values should be used as a starting point.
- Signal traces between the XTAL/EXTAL pins, the crystal, and the external capacitors must be as short as possible; these traces pins should only be connected to required oscillator components and must not be connected to any other devices or components. The connection between the MCU and the external oscillator should not have more than a single via with its the ground-via. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI.
- Keep other digital signal lines, especially clock lines, analog and frequently switching signal lines, as far away from the crystal connections as possible. Crosstalk from the digital activities may affect the small-amplitude of the oscillator signal.
- A ground area should be placed under the crystal oscillator area. This ground plane must be clean ground connected to the VSSx reference of the S32M2XX MCU. Never connect the ground guard ring to any other ground signal on the board. Also avoid implementing ground loops.
- The main oscillation loop current is flowing between the crystal and the load capacitors. This signal path (crystal to C_{XTAL} to $C_{EXTAL}$to crystal) should be kept as short as possible and should have a symmetric layout. Hence, both capacitor's ground connections should always be as close together as possible.

The following Figure 16 shows the recommended placement and routing for the oscillator layout.

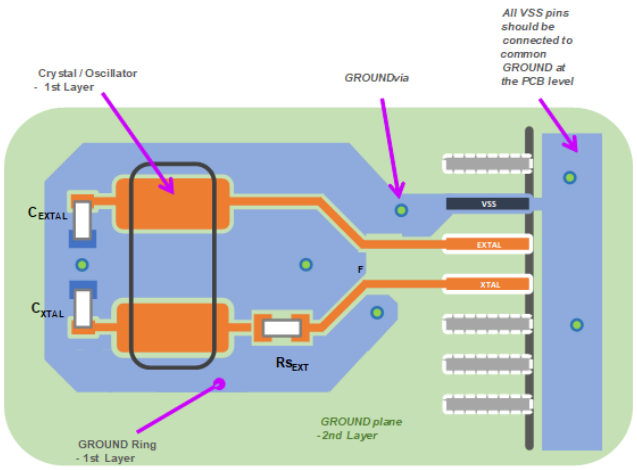


Figure 16. Suggested crystal oscillator layout

Based on the analysis and characterization of the oscillator manufacturer, the R_S and the values for C_{EXTAL} and C_{XTAL} can be adjusted or redefined in order to assure a safe oscillation margin.

To check and measure the crystal oscillation or any other signal characteristics, a frequency counter equipment is useful. Oscilloscopes and spectrum analyzers are generally not recommended because these types of equipment are usually not able to distinguish main oscillation from spurious, and the other hand, if the probes of the oscilloscope (despite that some probes are of low impedance) are connected directly to the oscillation circuit, it will stop and may affect or attenuate the crystal's oscillations.

7 GDU interface

The purpose of motor control is to maintain the speed, direction of rotation, or position of the motor shaft at desired level. This requires that the voltage applied to the motor is modulated in some manner. This is where the Power- MOSFET's play an important role. By turning the power-switching elements ON and OFF in a controlled way, the voltage applied to the motor can be varied in order to control the motor shaft's speed or position.

The S32M2xx contains an application extension with a GDU module. The GDU is a pre-driver designed for three-phase motor control applications. A combination of bootstrap circuit, charge-pump and boost converter enables to supply of high-side power MOSFETs of the H-Bridge. The boost converter maintains the voltage rails at safe levels when a low voltage input event occurs, while the bootstrap and

charge pump provides enough current to maintain bias voltage on the high side pre-driver section. The bootstrap circuit technique supplies the high instantaneous current needed for turning on the power devices.

7.1 FETs pre-driver interface

The pre-driver interface is connected directly to the external low-side and high-side power-MOSFETs. The primary function of a driver is to switch a MOSFET from off-state to on-state and vice versa. The pre-driver amplifies the control signals to the required levels to drive the power MOSFET. To guarantee reliable operation, the low-side drivers are supplied by the VLS regulator, while the high-side drivers are supplied directly by the bootstrap circuit over the VBS pins. The bootstrap diodes are integrated inside of the application extension die in order to reduce BOM. The maximum gate charge of power MOSFET supported by GDU is a maximum of 75nC.

7.1.1 S32M24XC Application - Block Diagram

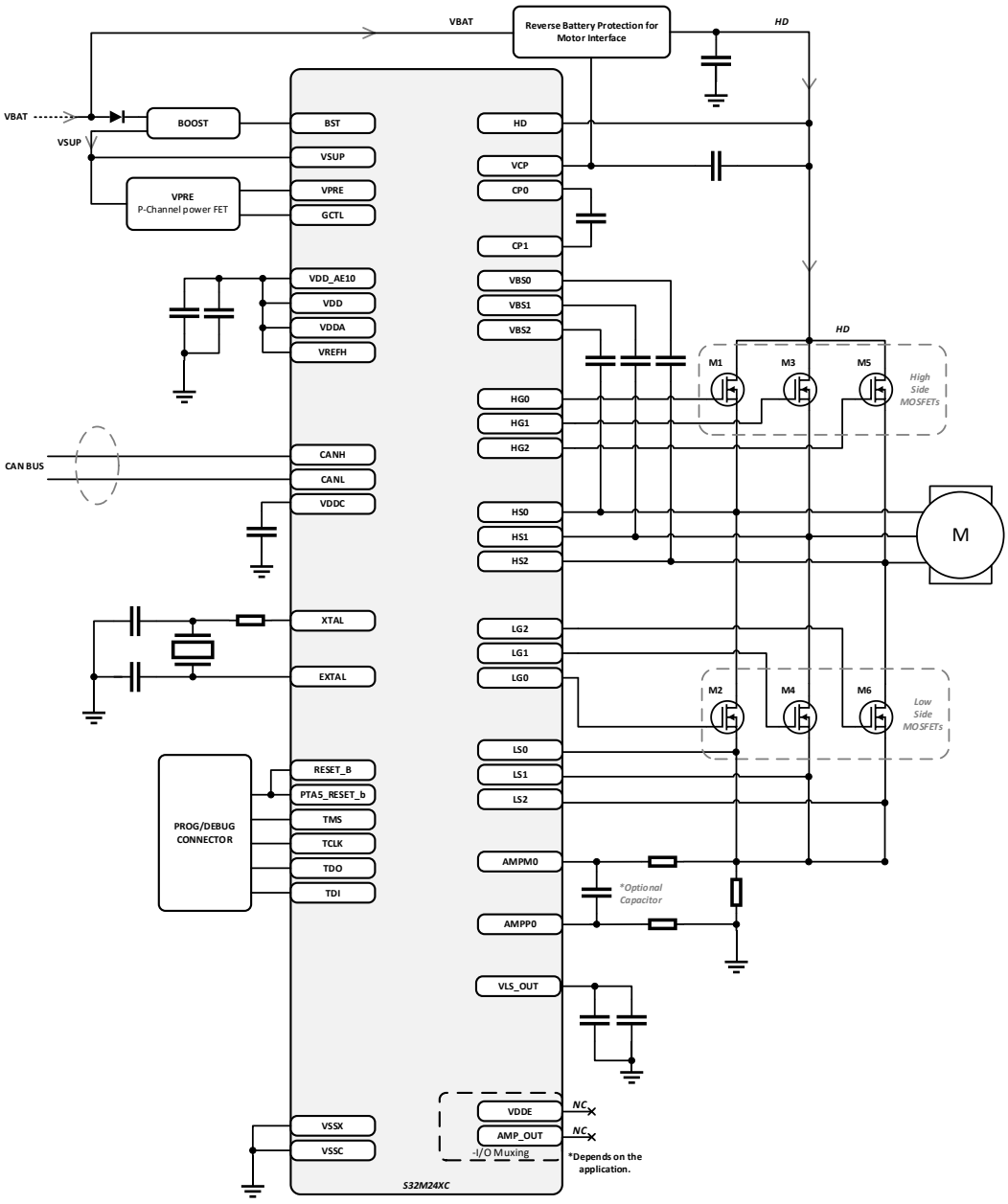


Figure 17. S32M24xC Application - Block Diagram

7.1.2 S32M24XL Application - Block Diagram

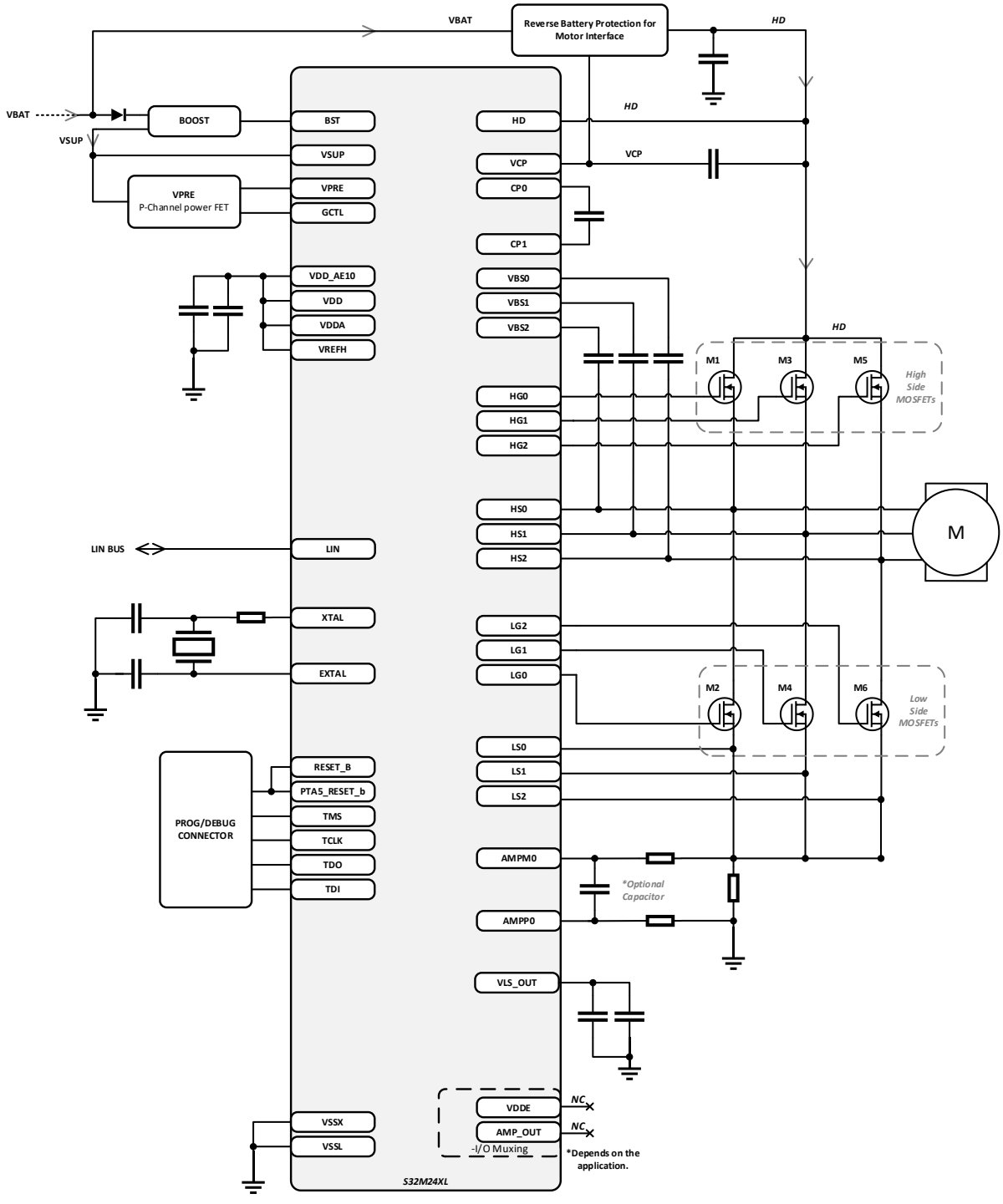


Figure 18. S32M24xL - Application Diagram

7.1.3 S32M27xC Application - Block Diagram

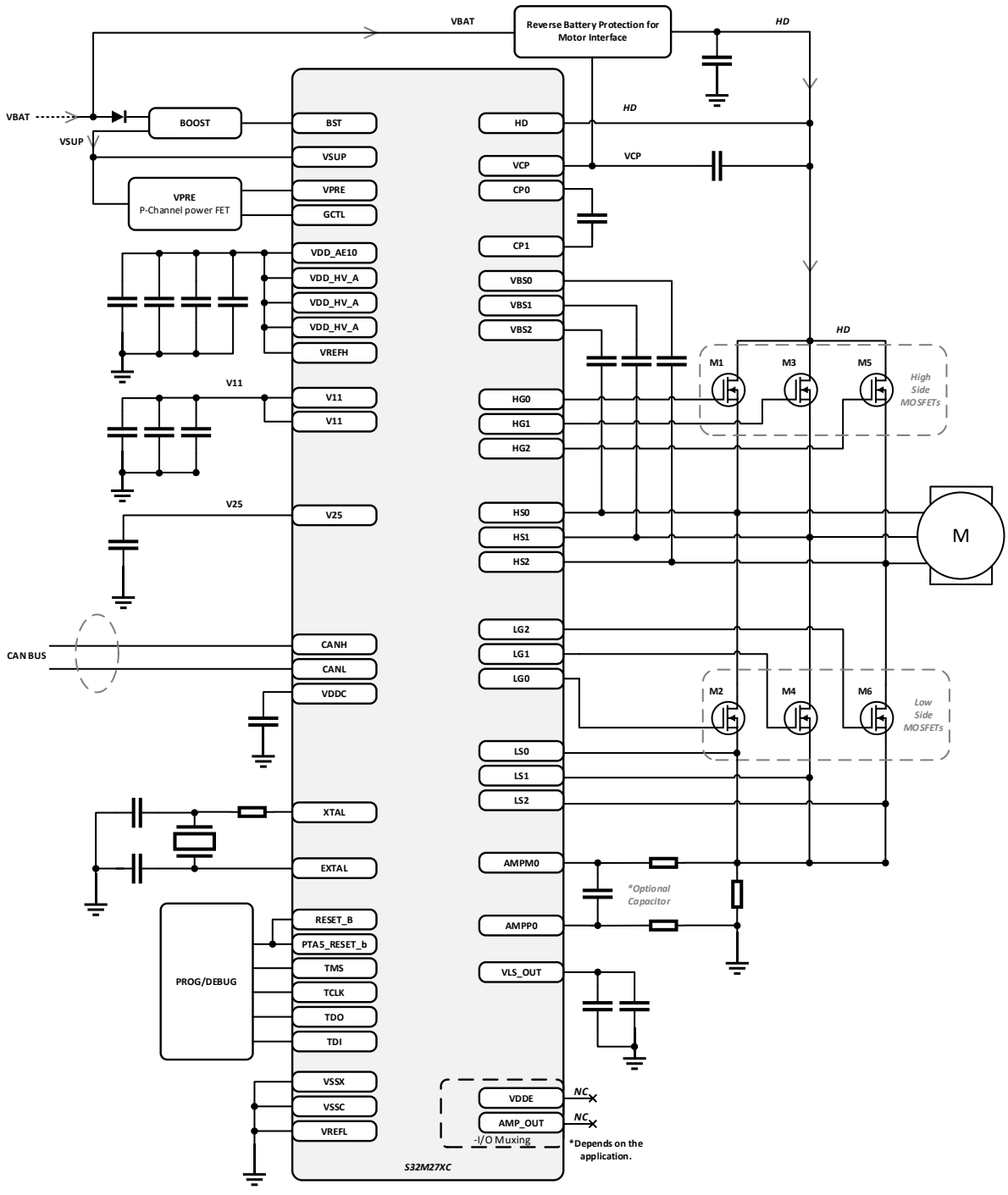


Figure 19. S32M27xC - Application Diagram

7.1.4 S32M27xL Application - Block Diagram

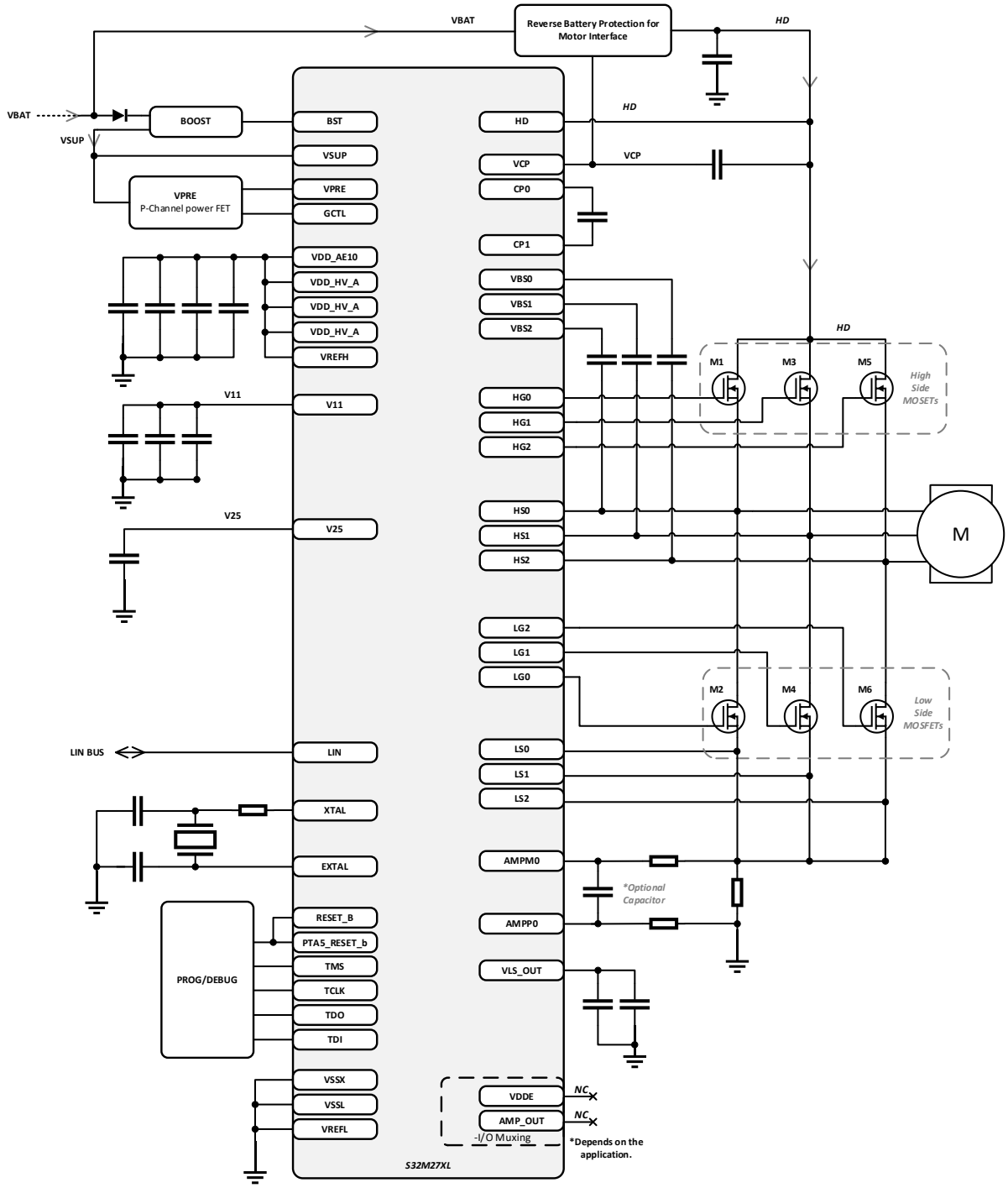


Figure 20. S32M27xL - Application Diagram

7.1.5 HD — FET pre-driver high side drain connection

This is the drain connection of the external high-side FETs. The GDU high-side drain voltage input, pin HD, is monitored within the GDU and mapped to an interrupt. In addition, this pin is connected to the ADC over voltage divider and enables measuring HD voltage level accurately. The HD pin should be connected as near as possible to the drain connections of the high-side MOSFETs. The HD pin must be protected with an external reverse battery protection circuit.

7.1.6 HG[2:0] — high-side gate pins

This pin is intended to supply the gate channel of high-side power MOSFET. The driver provides a high current with low impedance to turn on and off the high-side power FETs.

7.1.7 HS[2:0] — high-side source pins

This pin is intended to connect source channel of high side power MOSFET. In complementary connection of power MOSFETs, this pin is also connected to the drain of low side MOSFET. The low voltage end of the VBSx capacitor is also connected to this pin.

7.1.8 LG[2:0] — low-side gate pins

This pin is intended to supply gate channel of low side power MOSFET. The driver provides a high current with low impedance to turn on and off the low-side power FETs.

7.1.9 LS[2:0] — low-side source pins

This pin is intended to be connected to the source channel of low-side power MOSFET. The pins are usually connected through a shunt resistor in order to measure the MOSFETs current.

7.2 Selecting the power MOSFET

The dynamic characteristics of power MOSFETs determines the performance of the device. The total gate charge [QG], play an important role in the dynamic performance of the 3-phase MOSFET bridge. The charge on the gate terminal of the MOSFET is determined by its gate-to-source capacitance. Total gate charge, [QG], affects speed of power MOSFET switching, turn on and off. A lower gate charge means that higher switching frequency can be used. Operation at higher switching frequencies allows the use of allows to reduce DC-link capacitor values and DC-link inductors value, which can be significant factors in system cost. However, designers need to find balance between maximum allowable switching frequency and EMI/EMC.
The amount of charge necessary to switch the MOSFET can be determined from datasheet for particular gate-to-source voltage, drain current and drain-to-source voltage. Total gate charge can be also determined by formula below:

$$Q_G = I \times t$$

Equation 2.

Where:
Q_G= total gate charge number
I = gate current
t = device switching time

7.2.1 Switching process of the power MOSFET

The three phases during the turn-on period of power MOSFET with the corresponding drain to source voltage and drain current are depicted in Figure 21. Figure 24 shows the transition through these regions by means of output characteristics.

In the first period [S1], from t0 to t1, the MOSFET is turned off. Gate-to-source voltage [V_{GS}] rises from 0V to muller plateau voltage level [V_{GP}]. Once the applied gate-source voltage reaches the threshold voltage [V_{TH}], the MOSFET starts conducting drain current, and ID rises. In this phase, the gate current charges the input capacitance (CISS) with its V_{DS} clamped. MOSFET starts to conduct, and once the gate-source voltage reaches the muller plateau, the turn-on process enters the second phase.

In stage two [S2], from t1 to t2, the drain current finally reaches the level of the total load current. The gate-source voltage is clamped at V_{GP} level and remains relatively flat. During this region, the gate current is used to charge the reverse transfer capacitance (CRSS), and the MOSFET operates in the linear region. After the MOSFET takes over all of the load currents, the drain to source voltage V_{DS} starts to drop, and the circuit enters the third stage.

Switching losses start growing between the phase where the excitation gate-source voltage reaches threshold voltage V_{TH} and ends once drain-source voltage achieves threshold voltage V_{DSTH}. The minimum turn-on time is usually determined by the $\frac{dv}{dt}$ capability of the system. Reduction of the turn-on time causes an increase of the amount of diode reverse recovery current, and hence it causes an increase of the peak power dissipation. However, the total power losses tend to be reduced.

In stage three [S3], from t2 to t3, the MOSFET operation enters into Ohmic mode operation. Excitation gate-source voltage rises from V_{GP} to the driver supply voltage (V_{GDR}). Both I_D and V_{DS} remain relatively constant.

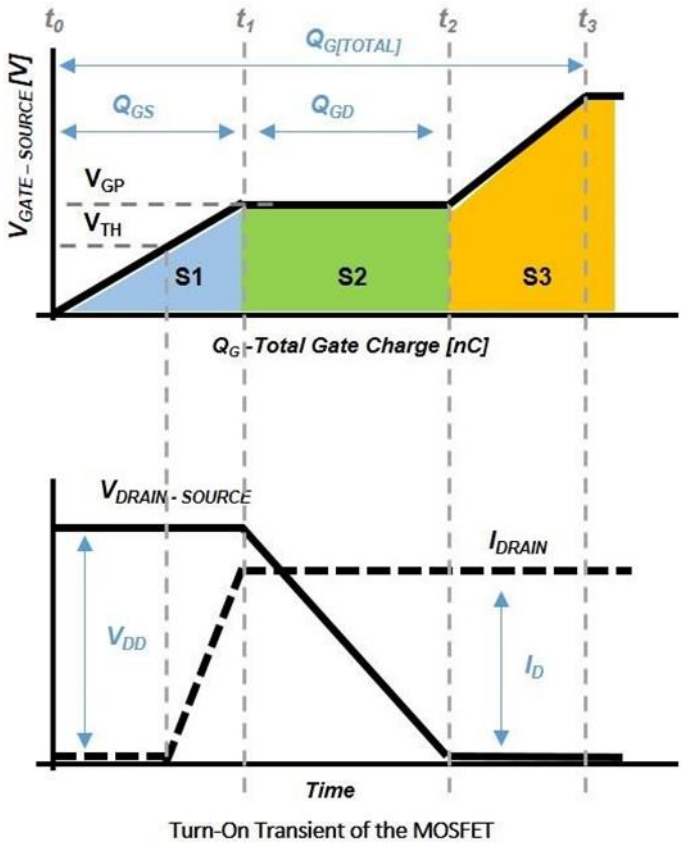


Figure 21. Gate-to-Source voltage and switching versus total charge

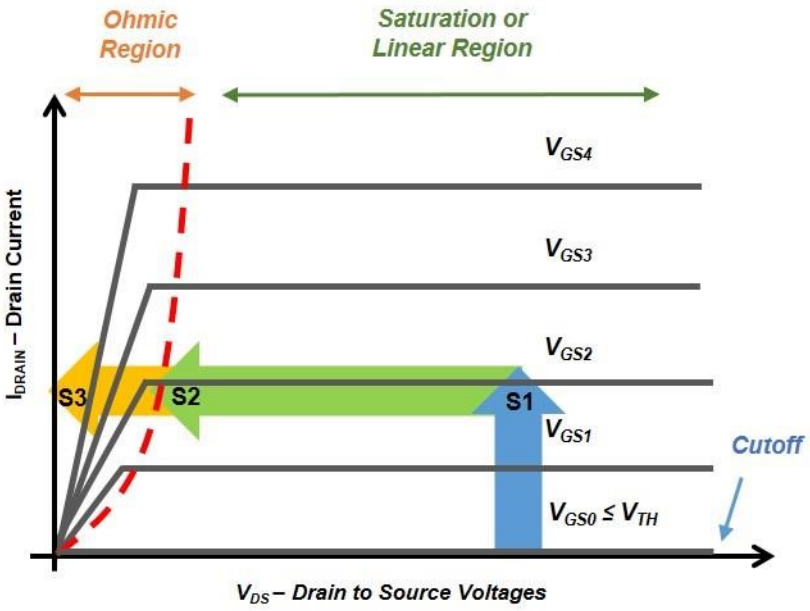


Figure 22. On-Region characteristics for different Gate-to-Source voltages

7.2.2 Internal diode reverse characteristic

For internal MOSFET diode, there is a requirement for this reverse recovery time [trr] to be as short as possible. The diode characteristics are essential if the MOSFET is used in the so-called "third quadrant". The third quadrant describes the operation of MOSFET, where the conduction role is taken over by the internal diode of MOSFET. This operation in the third quadrant of MOSFET is not continual it is only used during the deadtime period for complementary connected MOSFETs. Once the deadtime period has gone, the conduction role is taken over by MOSFET ohmic layer again. However, MOSFET internal body diode engagement, even for short time, causes growing of switching power losses (reverse recovery time trr) and growing of conduction losses (forward voltage of diode with dynamic resistance of diode). Diode reverse recovery time influences not only switching power losses but also causes oscillations which has direct impact to EMC/EMI.

7.2.3 Circuit layout considerations

The optimum switching performance of high-side and low-side gate drivers cannot be achieved without optimization of printed circuit board design. The precautions which must be taken into account in order to minimize the amount of stray inductance in the circuit are formulated as follows:

- The power MOSFET are placed as close as possible to the pre-driver interface of the S32M2xx microcontroller.
- Reduction of the length of traces to a minimum and using twisted pairs for all interconnections.
- For paralleled devices, keep all connections short and symmetrical.

7.3 Bootstrap circuit

A combination of bootstrap capacitors and a charge pump circuit are used for proper and sufficient excitation of high-side MOSFETs of the H-Bridge. The bootstrap capacitors deliver the high instantaneous current needed for turning the power devices on, while the charge pump provides enough current to maintain bias voltage on the upper driver sections and MOSFETs.

The high-side pre-driver must provide a sufficient gate-source voltage and sufficient charge for the gate capacitance of the external MOSFETs. The bootstrap capacitors are charged by means of a set of internal diodes. The gate of each device must be driven approximately 12V more positive than the supply voltage. To achieve this, an internal charge pump provides the gate drive voltage. For high-frequency applications, all bootstrap components are required.

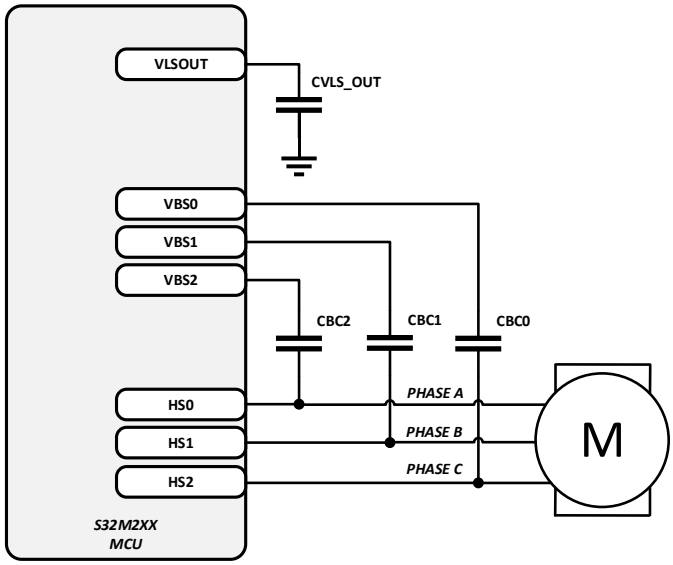


Figure 23. Charge pump circuitry

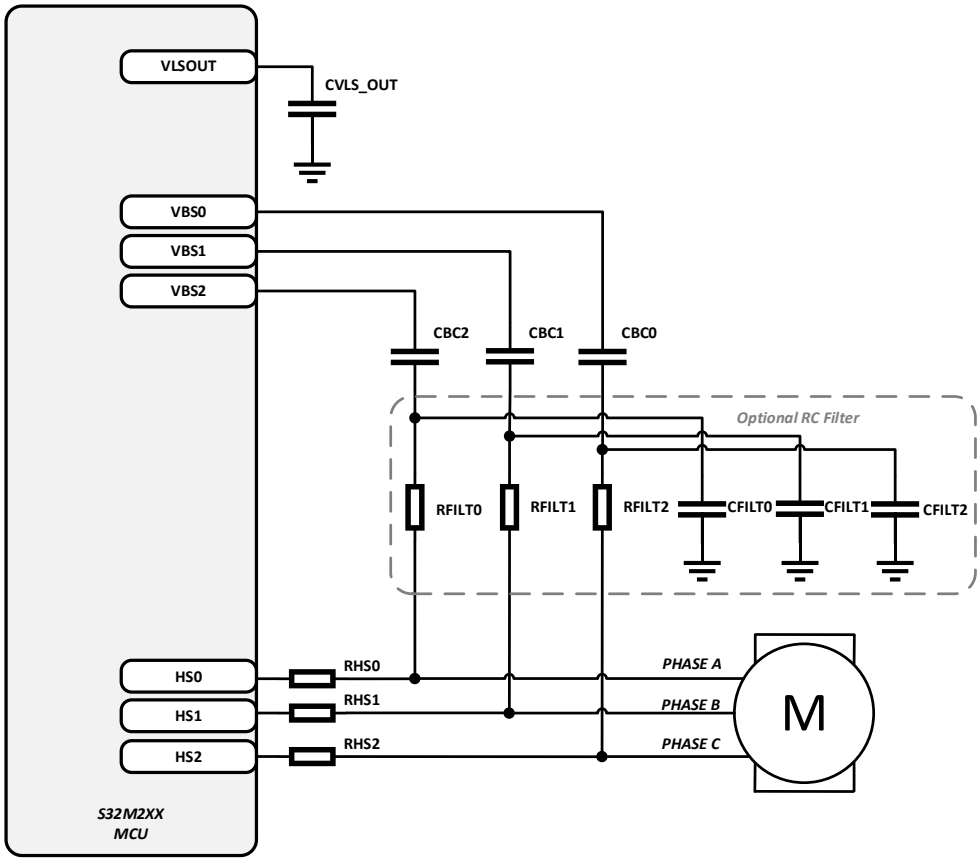


Figure 24. S32M2xx Charge pump circuitry with filter

Table 10. Recommended values for the bootstrap circuit.

Symbol	Description	Recommended Value	Comments
R_{FILTx}	Series resistor for filter purposes.	10 Ω	Optional
C_{FILTx}	Filter capacitors.	3.3 nF	
R_{HSx}	Series resistor for current limit.	10Ω	Mandatory
C_{CBx}	Filter capacitors. The value depends on the application	100 nF	Mandatory
$C_{VLS\ OUT}$	Bypass capacitor	2.2uF - 4.7uF	Mandatory
• VLS_OUT must not be used for external circuitry supply, this might cause unexpected behaviors.			

The capacitor is connected between HS[2:0] and VBS[2:0]. The bootstrap capacitor provides the gate voltage and current to drive the gate of the high-side MOSFET.

7.3.1 Printed circuit board

The layout for minimizing parasitic inductances is as follows:

- Direct tracks between MOSFET with no loops or derivation.
- Avoid interconnecting links. These can add significant inductance by lowering package height above the PCB

7.4 Charge Pump

An internal charge pump voltage is used to supply the high-side MOSFET pre-driver with enough current to maintain the gate-source voltage. To generate this voltage, an external capacitor is needed between the pins CP and CP1. The CP1 pin is the charge & discharge node. The pumped voltage is then available on the pin VCP.

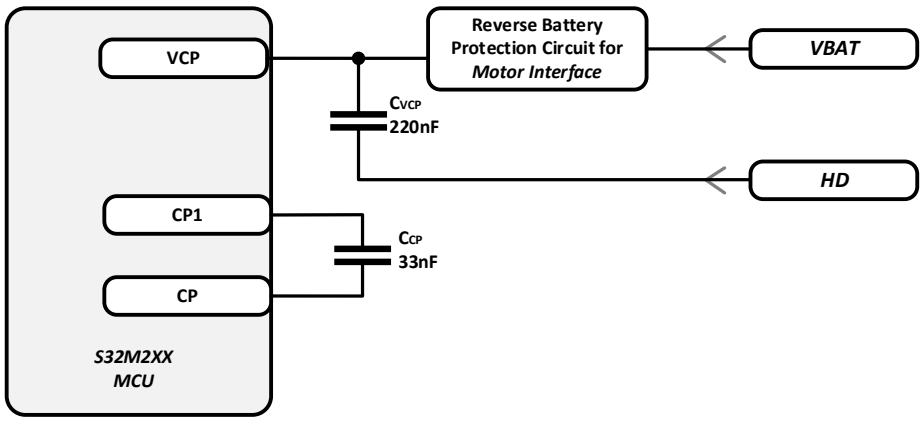


Figure 25. S32M2xx Charge Pump circuit

The CP/CP1 - Charge & discharge node for the MOSFET's charge pump pre-driver. These pins are connected to an external capacitor to make the charge pump circuitry work correctly.
The VCP - MOSFET pre-driver charge pump driver output pin is the pumped output signal that supplies the high-side MOSFET pre-driver supply VBS[2:0]. All the configurations for the charge pump driver can be accessed by the CPCFG register.

7.5 Boost converter

The GDU module in the S32M2XX integrates a controller to implement a boost converter. This module implements a switch which is controlled by a selectable frequency of the bus. There is a setup circuit for the boost converter.

Connect VBAT as the input voltage to the boost converter; an additional diode as VBAT reverse protection is required. See

- Figure 26.

7.5.1 BST — boost converter pin

This pin provides the essential switching elements required to implement a boost converter for low battery voltage conditions. This requires external diodes, capacitors, and a coil.

7.5.2 Diode Rectifier Selection

The rectifier must be capable of handling the capacitor's peak input current and of dissipating the rectifier's average power the rectifier voltage drop times the load current. The voltage breakdown of the device must be greater than the output voltage plus some margin. The typical choice for a rectifier in applications with low output voltage is a low-capacitance schottky diode. If the output voltage is high, a fast-recovery diode is an alternate possibility. For converters operating in CCM, a diode with a soft-recovery characteristic will minimize EMI.

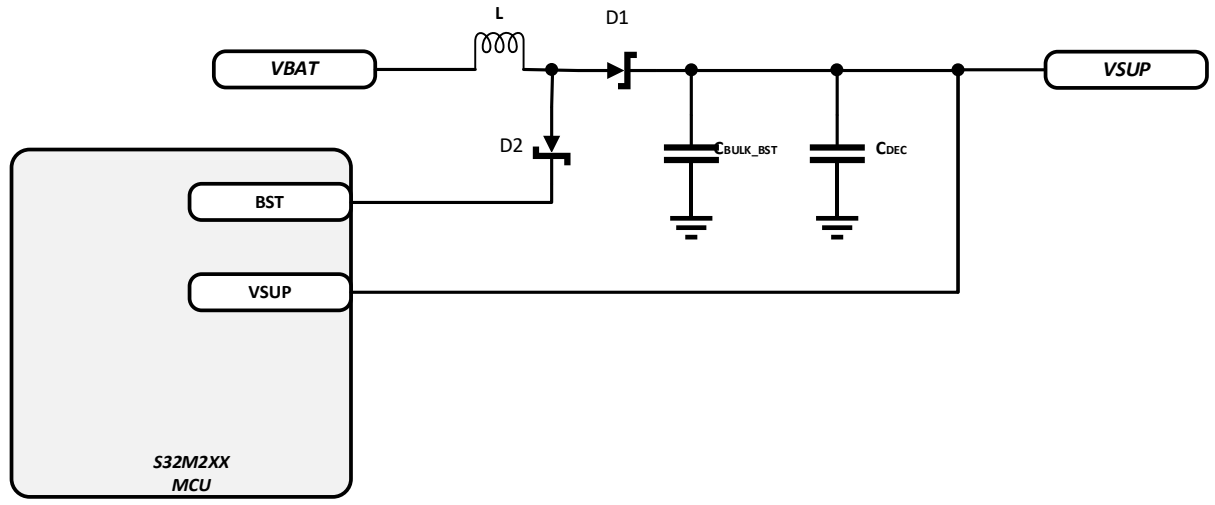


Figure 26. S32M2xx Options of the Boost circuitry

Table 11. Recommended values for the Boost converter circuit.

Symbol	Description	Recommended Value
L	Inductor	100 mH
C_{BULK_BST}	Local Bulk/Bypass Capacitor for domain	4.7uF - 10uF
C_{DEC}	Decoupling Capacitor	100nF - 220nF
D_{BST1}, D_{BST2}	Schottky Diode	-

The boost converter clock which is driving the transistor T1 is derived from the bus clock. This clock can be divided down as described in boost chapter in the reference manual. The boost converter also includes a circuit to limit the current through coil. This current limit can be adjusted with the bits BOCL[3:0] in the BOOSTCFG register.
When the internal transistor is connected to the ground, the diode D1 is reverse biased and the current flowing through the coil is increasing and the energy is stored in the coil. When the transistor is switched off the current flows through the diode and is charging up the capacitor. The coil current is decreasing and the voltage on the coil is inverted which leads to a higher output voltage .

The output voltage of the boost converter on VSUP pin is divided down and compared with a reference voltage [Vref] . As long as the divided voltage VSUP is below Vref the boost converter clock is enabled assuming that GBOE (GDU Boost Option Enable) is set.

8 DPGA

The Digital Programmable Gain Amplifier is integrated into the S32M2XX microcontroller for low-side current measurements. The interface consists of one digital programmable current sense amplifier with internal gain settings, blanking time counter and over-currents comparator. It senses voltage drop over the current sense resistor R_{sense}.

- The AMPP0 — Current Sense Amplifier Non-Inverting Input Pin.
- The AMPM0 — Current Sense Amplifier Inverting Input Pin.

DPGA amplifies the voltage drop corresponding to the load current so that it can be measured more precisely than non-amplified signal. The DPGA has the following features:

- A programmable amplification by 8, 16, 24, 32, 40, 50, 65, or 80.
- Differential input that allows both unipolar (only positive) and bipolar (both positive and negative) input voltage ranges.
- Configurable input common voltage.
- Configurable output common voltage.
- Blanking time, used to protect the amplifier against saturation.
- Voltage monitoring, used to generate an interrupt when the measured input voltage is out-of-bounds. You can configure the upper and lower limits of the allowed voltage range.
- Functional self-test for the amplifier and the voltage monitoring.

Proper operation of DPGA is conditioned to the appropriate configuration of DPGA registers listed in the RM.

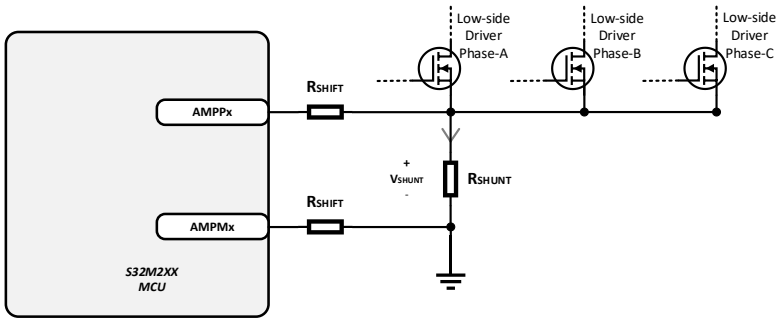


Figure 27. S32M2xx Current sense amplifier interface

In order to adjust the common voltage of the differential signal on the input, the interface in Figure 27 is required. The following rules are used for selecting the resistors in this circuit:

- The range for the R_{SHIFT} resistor must be between 5.1 kΩ and 2.34kΩ. Otherwise, it cannot limit the current drawn from/injected into the pin.
- The shifting voltage should cover the largest normal negative voltage on the terminal of the shunt resistor. It will not cover the negative voltage spikes.
- The shifting voltage should be less than 600mV.

The AMPCFG register can access all the configurations for the current sense amplifier interface diver.

8.1 Shunt resistor - design considerations

Shunt resistors are the most versatile and cost-effective means to measure the current. Selection of an appropriate shunt resistor depends on many factors, because its parameters can affect the current sensing performance.

The ideal resistors is only represented by resistive part, but real shunt resistor consists of parasitic inductance and capacitance. Parasitic inductance in AC or switching applications can cause unwanted couplings and high oscillations between the shunt resistor and the amplification circuit. The simulations of this network model can help to understand how to design current sensing circuit and avoid unwanted behaviors.

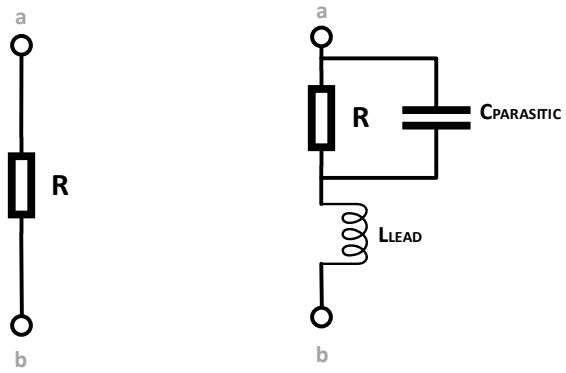


Figure 28. Ideal shunt resistor and real shunt resistor model.

The maximum ambient temperature has to be taken into account if we would like to calculate shunt resistor power dissipation.

Example:

This example considers the electrical characteristics of a shunt resistor BOURNS-BR3FB10L0 and the fictional requirements of current and temperature.

Assumptions:

- I_{MAX} = *16Amps*
- R_{SENSE} = *10mΩ @ 5W*
- $Tamb_{MAX}$ = *+150°C*

Analysis:

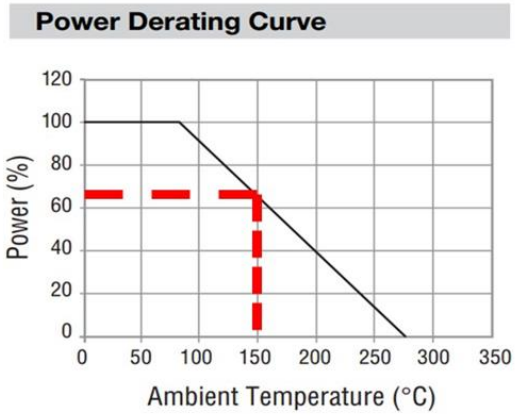


Figure 29. Power Derating Curve for - BOURNS- BR3FB10L0 part

Equation 5

$$PwrMAX = (16\ Amp)^2 \times 10m\Omega\ =\ 2.56W$$

Operation of the system at ambient temperature 150°C causes reduction of shunt resistor power rating to 65% of nominal power rating, then the maximum power dissipation allowed (to +150°C) is estimated as follows.

Equation 6

$$Pwr\_max + 150°C\ =\ 5W \times 0.65\ =\ 3.25W$$

The maximal dissipated power of shunt resistor operated in ambient temperature 150°C is 3.25W. The maximum generated power loss of shunt resistor for 16A is 2.56W. This shunt can be used and can operate in such conditions, because maximum dissipated power doesn't exceed tolerance for operation at 150°C ambient.

9 CAN physical layer

The physical layer characteristics for CAN are specified in ISO-11898-2. This standard specifies the use of cable comprising parallel wires with an impedance of nominally 120 Ω (95 Ω as minimum and 140 Ω as maximum). The use of shielded twisted pair cables is generally necessary for electromagnetic compatibility (EMC) reasons, although ISO-11898-2 also allows for unshielded cable. A maximum line length of 40 meters is specified for CAN at a data rate of 1 Mb. However, at lower data rates, potentially much longer lines are possible. ISO-11898-2 specifies a line topology, with individual nodes connected using short stubs.

Though not exclusively intended for automotive applications, CAN protocol is designed to meet the specific requirements of a vehicle serial data bus: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth. Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations. A typical CAN system with a S32M microcontroller is shown in Figure 30.

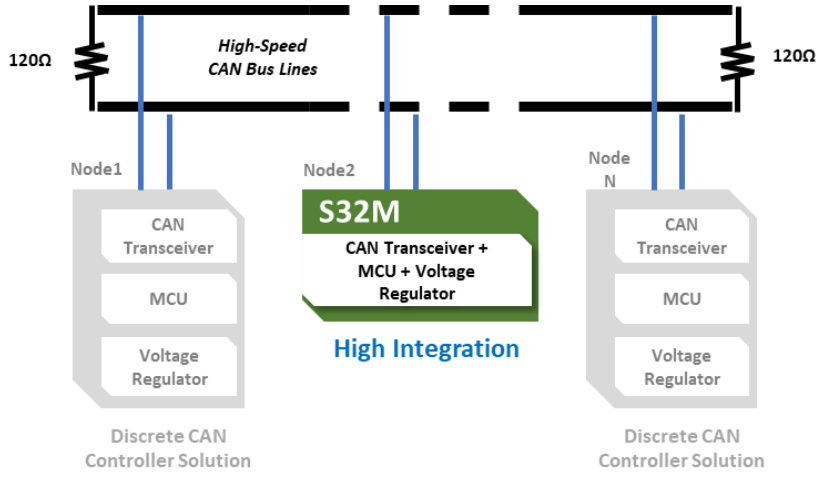


Figure 30. S32M2xx CAN system

The S32M2XX family contains an on-chip CAN physical transceiver and a dedicated power supply using an external power MOSFET. Having these modules on-chip helps reduce the total amount of components required to implement CAN communication.
Like most others CAN physical transceivers, the CANH, CANL pins are available for the designer to terminate bus depending on the application. The Figure 31 and Figure 32 show examples of the CAN node terminations.

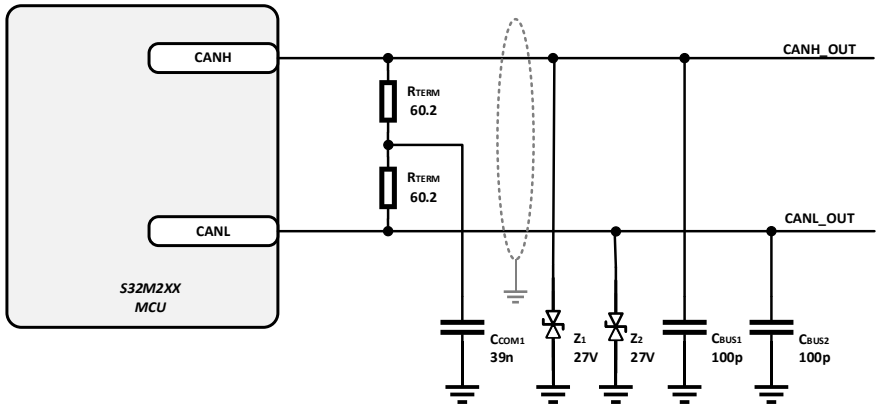


Figure 31. S32M2xx CAN physical transceiver circuit

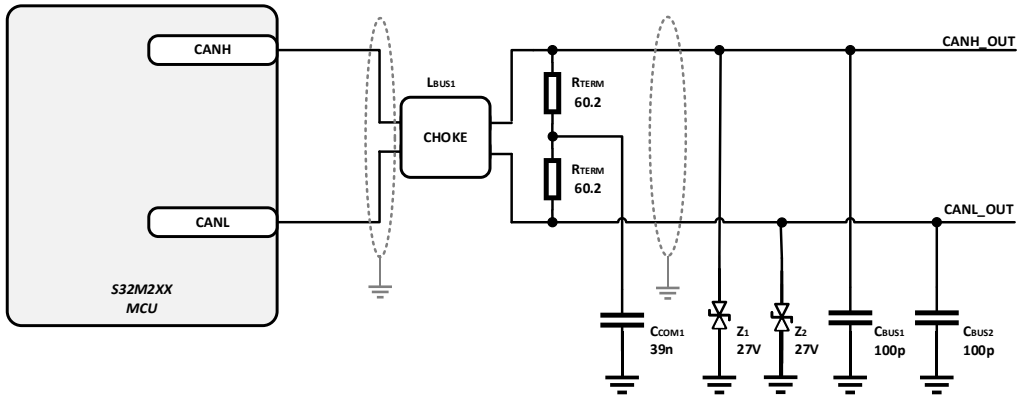


Figure 32. S32M2xx CAN Physical transceiver circuit with common mode choke

9.1 CAN components data

Table 12. CAN components

Reference	Description
	Denotes a guard track next to a high/medium speed track. Guard tracks are connected such that each end of the track is connected to ground. A guard track should be connected to the ground plane at least every 500 mils. Spacing from any protected conductor and the guard track must not exceed 20 mils.
C_{BUS1} and C_{BUS2}	The Capacitors C_{BUS1} and C_{BUS2} are not specifically required. They may be added for EMC reasons, in which case the maximum capacitance from either bus wire to ground must not exceed 300 pF total. If zener stacks are also needed, the parasitic capacitance of the zener stacks must also be included in the total capacitance budget.
Z1 and Z2	The zener stacks Z1 and Z2 could be required to satisfy Automotive EMC requirements (ESD in particular). These devices should be placed close to the connector.
R_{TERM1}, R_{TERM2} and C_{COM1}	Depending on the position of the node within the CAN network it might need a specific termination. R_{TERM1}, R_{TERM2} and CCOM1 they assist in having an overall cable impedance. On a

	bus implementation of a CAN network only the two nodes on the two ends of the bus have terminator resistors. The nodes which are not placed on the end of the CAN bus do not have termination. A thorough analysis is required to maintain this requirement of the CAN networks. The SPLIT pin on the transceiver is optional and the designer might choose not to use it. This pin helps stabilize the recessive state of the CAN bus and can be enabled or disabled by software when required.
LBUS1–Common mode choke	A common mode choke on the CANH and CANL lines can help reduce coupled electromagnetic interference and needed to satisfy Automotive EMC requirements. This choke, together with transient suppressors on the transceiver pins can greatly reduce coupled electromagnetic noise, and high frequency transients. LBUS1 is not specifically required.

9.2 Parallel termination

In CAN applications, both ends of the bus must be terminated because any node on the bus may transmit/receive data. Each end of the link has a termination resistor equal to the characteristic impedance of the cable, although the recommended value for the termination resistors is nominally 120 Ω (100 Ω as minimum and 130 Ω as maximum).
There should be no more than two terminating resistors in the network, regardless of how many nodes are connected, because additional terminations place extra load on the drivers. ISO-11898-2 recommends not integrating a terminating resistor into a node, but rather attaching standalone termination resistors at the furthest ends of the bus. This enables to avoid a loss of a termination resistor if a node containing such resistor is disconnected. The concept is also useful and enables to avoid the connection of more than two termination resistors to the bus, or locating termination resistors at other points in the bus rather than at the two ends.

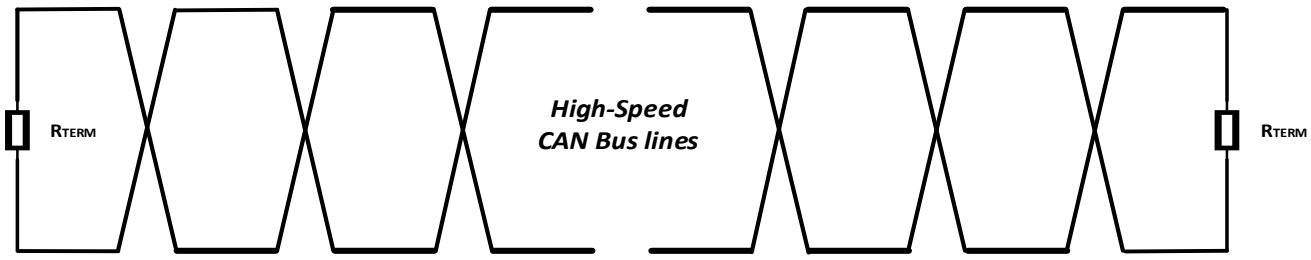


Figure 33. CAN Bus - parallel termination

9.3 Parallel termination with common-mode filtering

To further enhance signal quality, split the terminating resistors at each end in two and place a filter capacitor, C_{TERM}, between the two resistors. This capacitor filters unwanted high-frequency noise from the bus lines and reduces common-mode emissions. The value for this capacitor can vary between 4.7 nF and 100 nF, this capacitor and resistor are used as a low-pass filter.

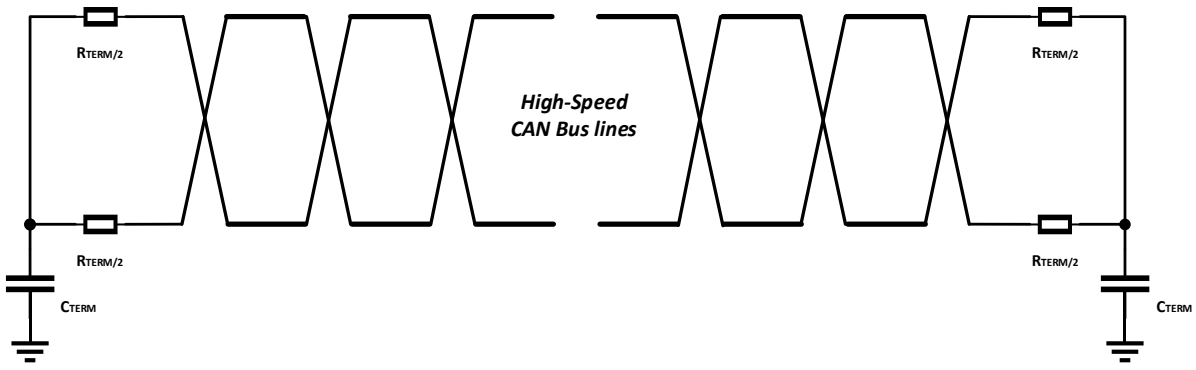


Figure 34. CAN Bus – parallel transmission with common-mode filtering

10 LIN Interface Circuit

The Local Interconnect Network (LIN) is a serial communication protocol, designed to support automotive networks. As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required.

The LIN Physical Layer module includes the following distinctive features:

- Compliant with LIN Physical Layer 2.2 specification.
- Compliant with the SAE J2602-2 LIN standard.
- Standby mode with glitch-filtered wake-up.
- Slew rate selection optimized for the baud rates: 10.4 Kbit/s, 20 Kbit/s and Fast Mode (up to 250 Kbit/s).
- Switchable 34 kΩ/330 kΩ pull up resistors (in shutdown mode, 330 kΩ only)
- Current limitation for LIN Bus pin falling edge.
- Overcurrent protection.
- LIN TxD-dominant timeout feature monitoring the LPTxD signal.

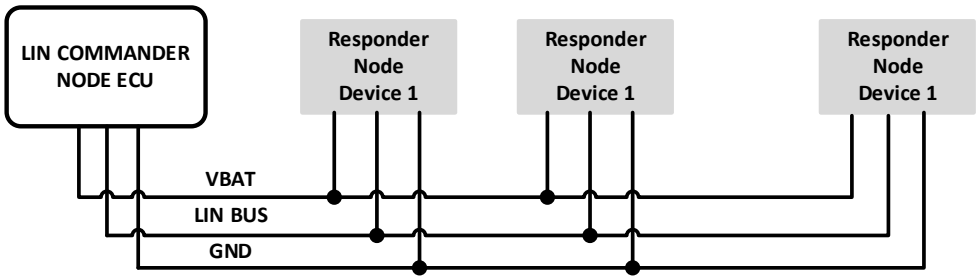


Figure 35. LIN Bus topology

The LIN transmitter is a low-side MOSFET with current limitation and overcurrent transmitter shutdown. A selectable internal pull up resistor with a serial diode structure is integrated, so no external pull up components are required for the application in a responder node. To be used as a commander node, an external resistor of 1 kΩ must be placed in parallel between VLINSUP and the LIN Bus pin, with a diode between VLINSUP and the resistor. The fall time from recessive to dominant and the rise time from dominant to recessive is selectable and controlled to guarantee communication quality and reduce EMC emissions. The symmetry between both slopes is guaranteed.

NOTE

According to the maskset of the S32M2XXL the reference of the LIN Physical Layer´s power supply can vary from HD or VSUP. Please refer chapter “Device Overview” in the Reference Manual.

Typical applications for LIN include switches, actuators (e.g., window lift and door lock modules), body control electronics for occupant comfort (e.g., door, steering wheel, seat and mirror modules), motors, and sensors (e.g., in climate control, lighting, rain sensors, smart wipers, intelligent alternators and switch panels).

The LIN bus topology utilizes a single commander and multiple nodes, as shown below. Connecting application modules to the vehicle network makes them accessible for diagnostics and service.

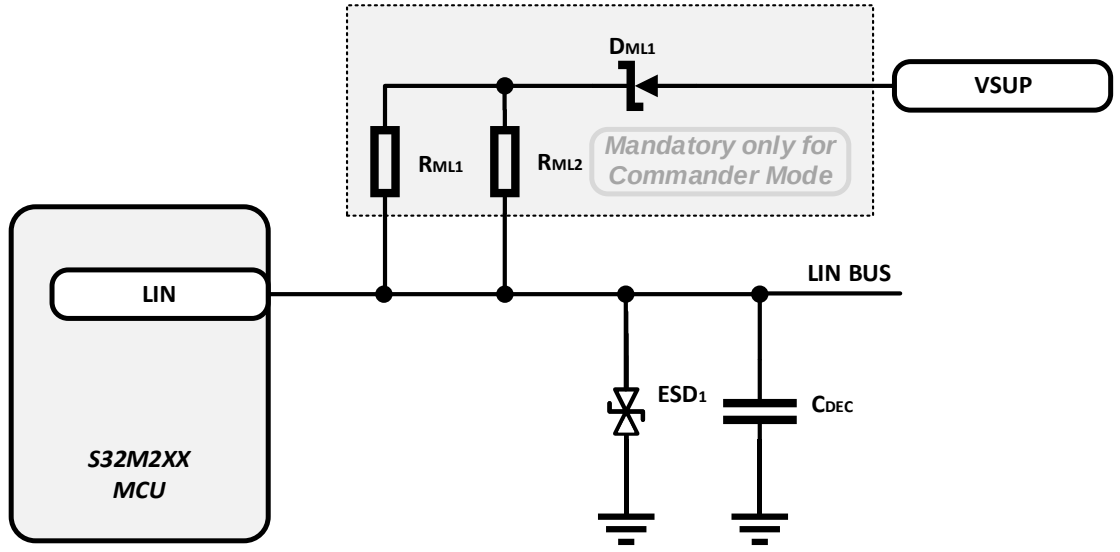


Figure 36. S32M2xx Circuit diagram for LIN interface

10.1 LIN components data

Table 13. LIN components

Reference	Part	Mounting	Remark
D_{MLIN}	Diode	Mandatory only for commander ECU	Reverse Polarity protection from LIN to VSUP.
R_{ML1} , R_{ML2}	Resistor: 2 kΩ Power Loss: 250 mW Tolerance: 1% Package Size: 1206 Requirement: Min Power rating of the complete commander termination must be ≥500nW	Mandatory only for Commander ECU	For Commander ECU If more than 2 resistors are used in parallel, the values have to be chosen in a way that the overall resistance RM of 1 kΩ and the minimum power loss of the complete commander termination has to be fulfilled. For Responder ECU R_{MLIN1} and R_{MLIN2} are not needed on the PCB layout
C_{DEC}	Capacitor: Responder ECU: typically, 220 pF Commander ECU: from 560 pF up to approximately ten times that value in the responder node [$C_{RESPONDER}$], so that the total line capacitance is less dependent on the number of responder nodes. Tolerance: 10% Package Size: 0805 Voltage: ≥50 V	Mandatory	The value of the commander node has to be chosen in a way that the LIN specification is fulfilled.
ESD_1	ESD Protection Package Size: 0603-0805	Highly recommended	Layout pad for an additional ESD protection part. Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.

11 Unused pins

Unused digital pins can be left floating. To reduce power consumption, it is recommended that these unused digital pins are configured as inputs and have the internal pull resistor enabled. This will decrease current consumption and susceptibility to external electromagnetic noise. ADC unused pins should be grounded to reduce leakage currents.

The following table describes the options and configurations for the unused pins and the considerations for other modules and sections of the MCU.

Table 14. S32M2xx - Unused pins configuration

Module	Pin Name	Function	Recommendation
GPIO	PTx[1]	FTMx	The unused pins should be left unconnected, or externally connected to VSS/GND. [2] [3]
		FlexIOx	
		CANx	
		LPUARTx	
		LPI2Cx	
		ADCx	
		CMPx	
		Others	
	PTB6	XTAL	The pins with the XTAL and EXTAL functions should be left unconnected, or externally connected to VSS/GND.[2] [3]
	PTB7	EXTAL	
JTAG	PTA4	JTAG_TMS/SWD_DIO	The pins with the JTAG function should be left unconnected. In order to increase debugger connection robustness, it is recommended to add external pull resistors in parallel to the internal weak pull-ups (TDI, TDO, and TMS) or pull-down resistors (TCK). Refer to Debug and programming interface.
	PTA10	JTAG_TDO/SW_DO	
	PTC5	JTAG_TDI	
	PTC4	JTAG_TCK/SWD_CLK	
RESET	PTA5	PTA5/RESET	Reset pins must always be shorted together externally to a common reference on PCB. Refer to the RESET system and Debug and programming interface.
	RESET_B	RESET_B	
POWER	VDDx	VDD	No Power pin should be left unconnected. VDD and VDD_A10/VDDA/VREFH must be shorted together externally to a common reference on PCB. Appropriate decoupling capacitors to be used to filter noise on the supplies. Refer to Power management.
	VDDA	VDDA	
	VDDC	VDDC	
	VDD_HV_A[5]	Main I/O and Analog Supply Voltage	
	VDD_AE10	VDD_AE10	
	VREFH	ADC High Reference Voltage	The positive reference should be connected to the same potential as VDD/VDD_A10/VDDA/VREFH or may be driven by an external source to a level between the minimum VREFH and the VDDA potential. VREFH must never exceed VDDA. Refer to Power management.
	V11[5]	Core logic voltage supply (+1.1 V)	No V11 power pin should be left unconnected. All V11 power pins must be shorted together externally on their voltage domain. Appropriate bulk/bypass and decoupling capacitors should be used to filter noise on the supply. Refer to Power management. The V11 domain must not be used or connected to other interfaces in the application.
	V25[5]	Flash memory supply (+2.5 V)	The V25 power pin should not be left unconnected; the decoupling capacitor should be used to filter noise on the supply. Refer to Power management. The V25 domain must not be used or connected to other interfaces in the application.
GROUND	VSSx	VSS	No Ground pin should be left unconnected. All VSSx and VSSC must be shorted together externally to a common GND.
	VSSC	Ground Pin for CAN Physical Layer.	
GDU	VPRE	Voltage Pre-Regulator	If not used the VPRE voltage regulator must be configured to operate with the internal power transistor by setting the appropriate register; VPRE internal regulator (VPREINT=1, VPREEXT=0) or using VPRE external regulator (VPREINT=0, VPREEXT=1).
	BST	MOSFET pre-driver boost converter connection	This pin should be left unconnected if the boost option is not required.
	AMPM0	DPGA	The pins with the AMPM0 and AMPP0 functions should be left unconnected.
	AMPP0		

1. Pins bonded and not bonded out.
2. For unused digital and analog pins, the pin function should be set to DISABLED by setting the corresponding
3. PORTx_PCRn[MUX] field to 0b000 only for the S32M24x devices and SIUL2x_IMCR[MUX] field to 0b000 for the S32M27x devices. The DISABLED function is default state for all pins not initialized. For pins with ADC functionality software should not trigger ADC channel conversion on the channel which is multiplexed with the unused pin. For pins with CMP functionality software should not enable CMP channel connected to the unused pin.
4. If the unused pin is connected to VDD or VSS, and the pin is unintentionally configured to output with a different state, then there could be a path that can increase current drastically and causes major damage in the MCU.
5. Only available on S32M27X.

12 General board layout guidelines

12.1 Traces recommendations

A right angle in a trace can causes more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in the Figure 37.

Figure 37. Poor and correct way of bending traces in right angles

If two layers are adjacent in a PCB stack-up, the routing must be wisely designed in order to fulfill specific requirements and avoid unwanted effects. The adjacent signal layers has to route in direction, where they are crossing each other's instead of being routed in parallel. If signal layer L_N is being routed "north-to-south," then make sure that L_{N+1} is being routed in direction "east-to-west." In this way, you can minimize the possibility of broadside coupling.

12.2 Grounding

Grounding techniques apply to both multi-layer and single-layer PCBs. The objective of grounding techniques is to minimize the ground impedance and thus to reduce the potential of the ground loop from circuit back to the supply.

To minimize crosstalk, Ground planes between two adjacent signal layers must be used to reduce the chance of broadside coupling even more. Not only will this increase the distance between the layers but also this configuration will give you a much better return path through the ground plane.

- Route high-speed signals above a solid and unbroken ground plane.
- If the high-speed signal requires to be routed on another layer by a via, therefore every time a via is utilized, a ground via should also be utilized next to the signal via. This allows to flow the return current near the signal current and minimize that the trace changes their impedance.
- Do not split the ground plane into separate planes for analog, digital, and power pins. A single and continuous ground plane is recommended.
- There should be no floating metal/shape of any kind near any area close to the microcontroller pins. Unused solid copper area of signal planes has to be grounded by means of via.

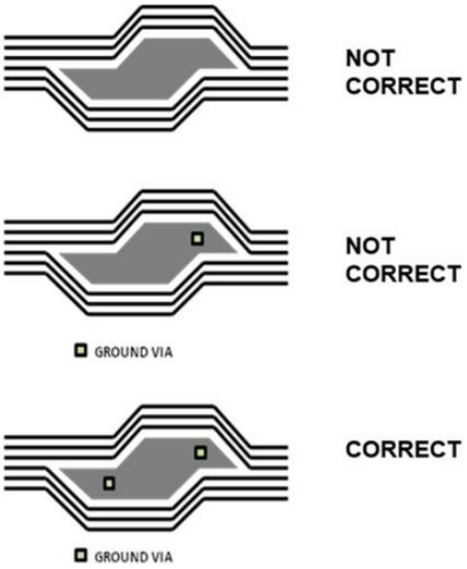
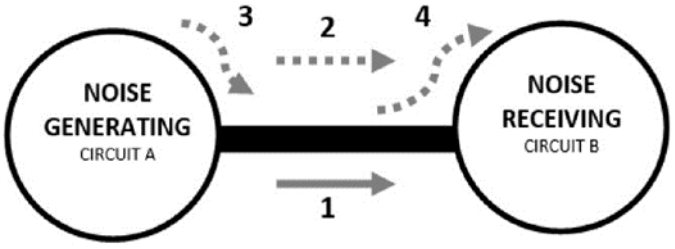


Figure 38. Eliminating floating metal/shape

12.3 EMI/EMC and ESD considerations for layout

These considerations are important for all system and board designs. Though the theory behind this is well explained, each board and system experience this in its own way. There are many PCB and component-related variables involved.

This application note does not go into the electromagnetic theory or explain why different techniques are used to combat that effects, but it considers the effects and solutions most recommended as applied to CMOS circuits. EMI is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby. Studying EMC for your system allows testing the ability of your system to operate successfully counteracting the effects of unplanned electromagnetic disturbances coming from the devices and systems around it. Electromagnetic noise or disturbances travels via two media: Conduction and Radiation.



	Propagation path
1	Conductor
2	Air
3	Air to Conductor
4	Conductor to Air

Figure 39. Electromagnetic noise propagation

The design considerations narrow down to:

- The radiated & conducted EMI from the board should be lower than the allowed levels by the standards you are following.
- The ability of the board to operate successfully counteracting the radiated & conducted electromagnetic energy (EMC)from other systems around it.

The EMI sources for a system consist of several components such as PCB, connectors, cables, and so on. The PCB plays a major role in radiating high-frequency noise. At higher frequencies and fast-switching currents and voltages, the PCB traces become effective antennas radiating electromagnetic energy; e.g., a large loop of signal and corresponding ground. The five main sources of radiation are digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast-switching clocks, external buses, and PWM signals are used as control outputs in switching power supplies. The switching mode power supply is another major contributor to EMI. RF signals can propagate from one section of the board to another building up EMI. Switching power supplies radiate energy that can fail the EMI test. This is a huge subject and there are many books, articles, and white papers detailing the theory behind it and the design criteria to combat its effects.
Every board or system is different as far as EMI/EMC and ESD issues are concerned, requiring its own solution.
However, the common guidelines to reduce an unwanted generation of electromagnetic energy are as shown below:

- Ensure that the power supply is rated for the application and optimized with decoupling capacitors.
- Provide adequate filter capacitors on the power supply source. The bulk/bypass and decoupling capacitors should have low equivalent series inductance (ESL).
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias.
- Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.

13 PCB layer stacking

The following layer stack-ups are recommended from four to teen-layer boards, although other options may be feasible.

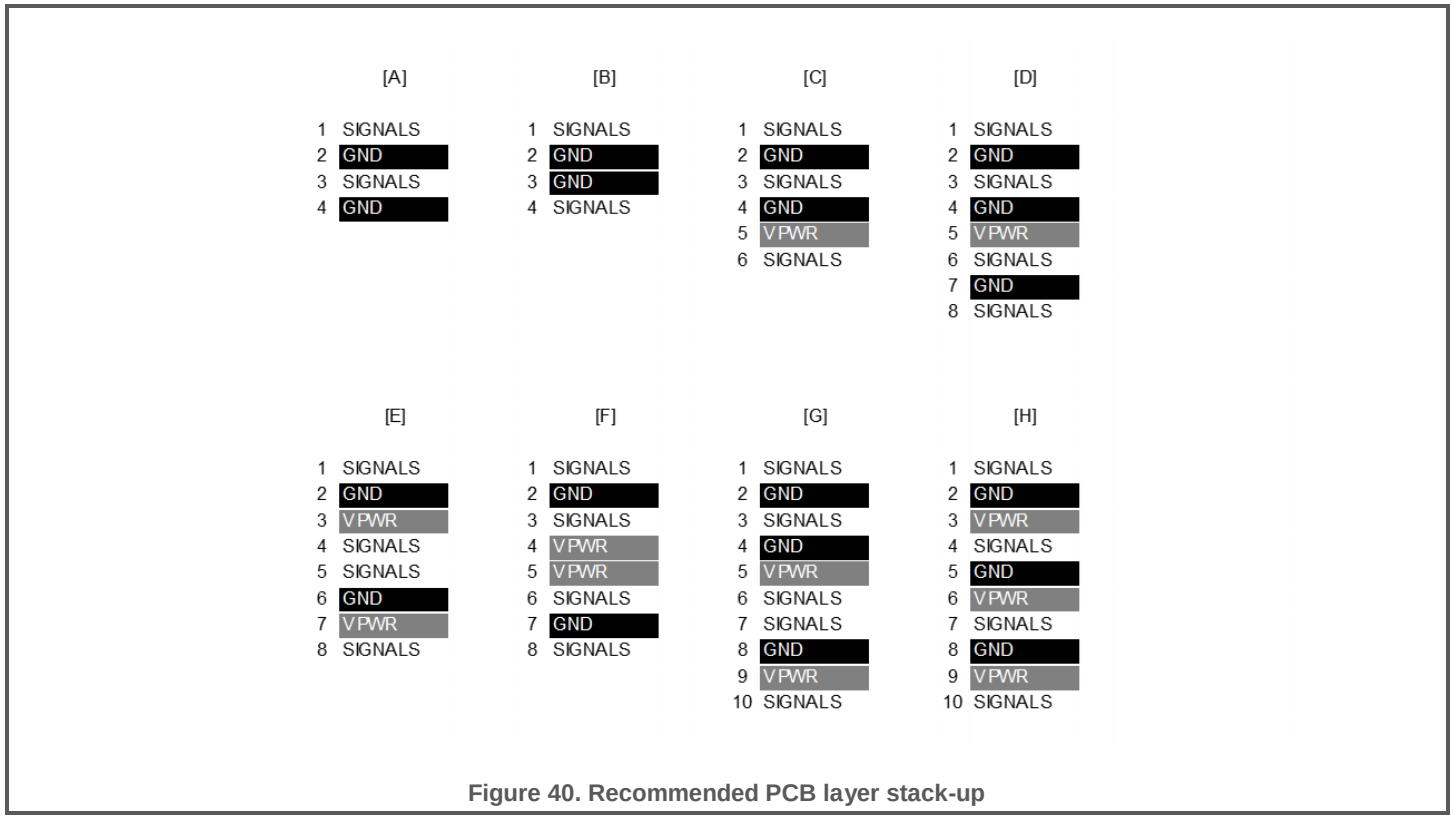


Figure 40. Recommended PCB layer stack-up

14 Injection current

The injection current damage in a microcontroller unit (MCU) port can occur when a pin is exposed to a high-current or a high-voltage signal. The consequences of injection current damage can range from temporary malfunctions to permanent MCU failure. Symptoms may include unpredictable behavior, data corruption, or system crashes. In the most severe cases, the MCU may become completely unusable, requiring replacement. To prevent injection current damage, it is essential to take protective measures, such as using appropriate grounding techniques and protective components like TVS diodes, EMI filters, and decoupling capacitors. These measures ensure the reliable operation of the circuit and minimize the risk of injection current damage

All pins implement protection diodes that protect against electrostatic discharge (ESD). These internal ESD diodes of the microcontroller are designed just for short discharge pulses only, and these do not sustain a constant current over time. Therefore, the maximum continuous voltage that drops over them is specified in the DC electrical parameters and the maximum high input voltage should not be higher than VDD_HVx + 0.3 V, and the current injection also should be limited as defined in the device datasheet. In other words, the voltage and current of an input signal must be within the electrical parameter allowed. The outcome of violating these specifications causes unexpected behavior, stuck operation or damage in the MCU.

When the MCU is in an unpowered state, current injected through the chip pins may bias internal chip structures (for example, ESD diodes) and incorrectly power up these internal structures through inadvertent paths. The presence of such residual voltage may influence different chip-internal blocks in an unpredictable manner and may ultimately result in unpredictable chip behavior (for example, POR flag not set). Once in the illegal state, powering up the chip further and then applying reset will clear the illegal state. Injection current specified for the chip under the aspect of absolute maximum ratings represent the capability of the internal circuitry to withstand such condition without causing physical damage.

14.1 Input circuits for automotive applications

The signal conditioning circuits are the one of most important sections of an electronic design, especially when it comes to safeguarding microcontrollers interfacing through their digital and analog ports with external signals. These circuits must be designed carefully, ensuring that signals are pristine, noise-free, compatible, and within the normal operation limits of the microcontroller. The vital role of the signal conditioning circuits for the microcontroller extends beyond signal enhancement, serving as a shield and protection against injection current damage and Electrostatic Overstress (EOS). In the next sections, it will be detailed some common circuit topologies used in automotive applications.

14.1.1 High Side switch - Level Shifter with Passive Resistors

A significant challenge is protecting the microcontroller from voltage spikes and injection current, specifically in scenarios where the input port is connected to a battery voltage. To address this challenge, the initial circuit integrates a combination of resistors, capacitors, and a Zener diode to offer protection against overvoltage and injection current.

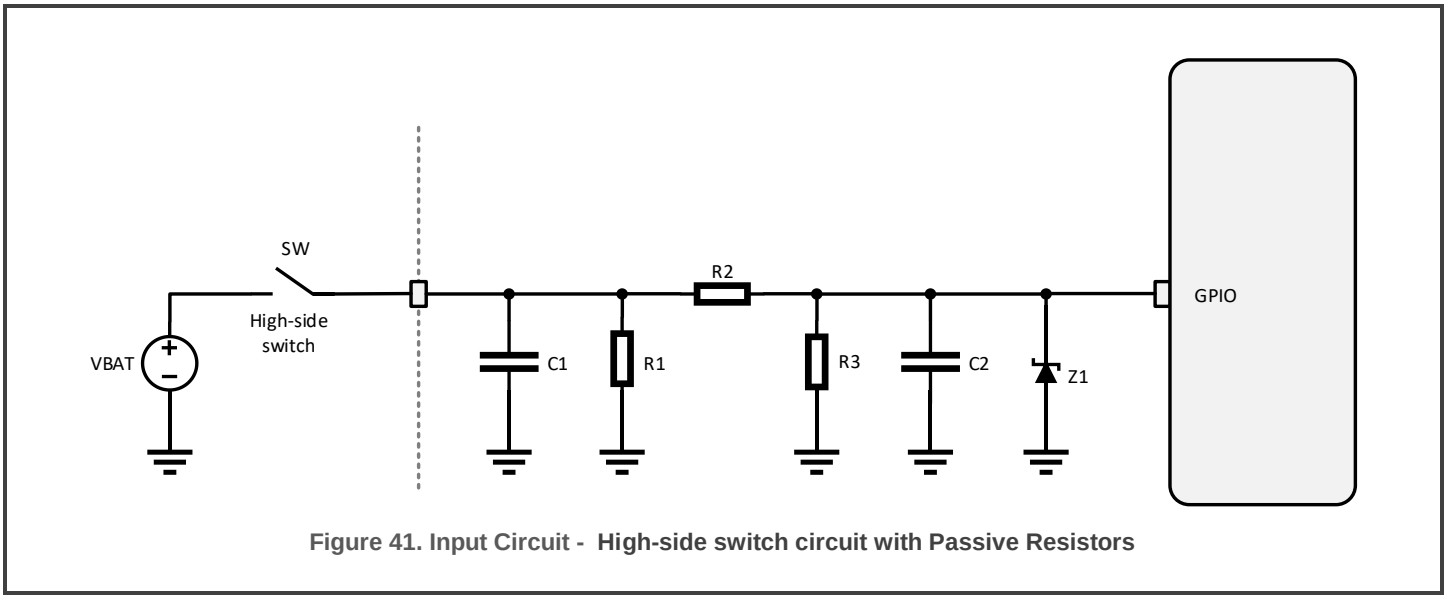


Figure 41. Input Circuit - High-side switch circuit with Passive Resistors

Table 15. Component description for the High-side switch circuit with Passive Resistors

Symbol	Description
C1	ESD protection and EMC filter
C2	EMC filter and low-pass filter in conjunction with R2‖R3 to filter input noise
R1	Primary load for the source switching device to provide wetting current for contacts and connectors. A low impedance also helps to reduce cross-talk
R2	Forms a voltage divider with R3. Limits current into the load and with R3, forms a low-pass filter with C2.
R3	Forms a voltage divider with R2
Z1	Zener diode to provide a protection against overvoltage

This circuit starts with an ESD/EMC protection capacitor at the input to prevent any high-voltage spikes from reaching the microcontroller's I/O pin. The voltage divider network with resistors is then used to lower the input voltage to a safe level for the microcontroller. The filtering capacitor after the voltage divider network further smooths the input signal, ensuring that any remaining noise or high-frequency signal is removed. Finally, the Zener diode provides a stable reference voltage to prevent any voltage spikes or any other voltage levels that exceeds the maximum normal operating voltage of the GPIO. The combination of the ESD/EMC protection capacitor, the voltage divider network with resistors, the filtering capacitor, and the Zener diode provide a robust protection mechanism for the microcontroller, ensuring safe and reliable operation in scenarios where a battery voltage is connected to its input port. This circuit provides a cost-effective solution to protect microcontrollers from overvoltage and injection current and can be implemented in a wide range of applications.
Overall, by utilizing these components, the circuit can effectively prevent injection current, voltage spikes, and other potentially harmful electrical events that could damage the microcontroller. As a result, this protection circuit is an essential element in ensuring the longevity and reliability of any electronic system incorporating a microcontroller.

14.1.2 High Side Switch - Level Shifter with a NPN Common Emitter Transistor

The circuit must be designed to protect a microcontroller port from injection current when a battery-level voltage is applied. It consists of a voltage divider using resistors, an ESD and EMC capacitor at the input, and a filtering capacitor after the voltage divider. Additionally, a diode is included to protect against reverse battery connection. The output of this circuit is connected to the base of a transistor in common emitter configuration, acting as a digital buffer switch.

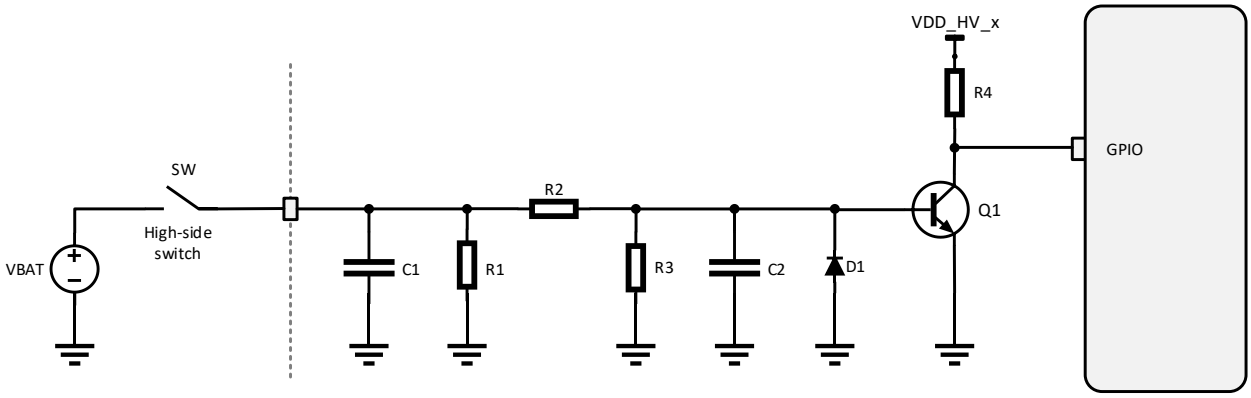


Figure 42. Input Circuit - High-side switch circuit with a NPN Transistor

Table 16. Component description for the High-side switch circuit with a NPN Transistor

Symbol	Description
C1	ESD protection and EMC filter
C2	EMC filter and low-pass filter in conjunction with R2‖R3 to filter input noise
R1	Primary load for the source switching device to provide wetting current for contacts and connectors. A low impedance also helps to reduce cross-talk
R2	Forms a voltage divider with R3. Limits current into the load and with R3, forms a low-pass filter with C2.
R3	Base-emitter bias resistor for Q1. Forms a voltage divider with R2. The resistor helps to keep the transistor off by shunting collector-base junction leakage current to ground.
D1	Reverse voltage protection for Q1's base-emitter junction.
Q1	Small-signal transistor to buffer the input and act as a digital switch.
R4	Load resistor for Q1.

The voltage divider circuit is used to reduce the battery voltage to a suitable level for the transistor's base. The ESD and EMC capacitor protects the circuit from electrostatic discharge and electromagnetic interference. The filtering capacitor removes any high-frequency noise from the input voltage, ensuring a clean DC signal for the transistor.

The transistor in common emitter configuration provides a high gain and a high input impedance, making it an ideal choice for buffering digital signals. The transistor is connected as an inverter, so when the input signal is high, the output is low, and vice versa. This arrangement ensures that the microcontroller's port is protected from any injection current that might be present in the input voltage.

14.1.3 Low Side Switch - Level Shifter with passive Resistors

To ensure the longevity and reliability of an automotive electronics system, it is essential to protect the input pin of an MCU from injection current and overvoltage. The following multi-stage protection circuit can be implemented to achieve this goal. The following circuit is designed to connect a switch to GND as the input and includes several stages. At the input, an EMI/ESD capacitor is used, followed by a pull-up resistor. This resistor is the primary load for the source switching device and provides wetting current for contacts and connectors, while also reducing cross-talk. Typically, the pull-up resistor is connected to a battery-protected voltage source. A voltage divider is used next to reduce the voltage to a suitable level for the MCU. This voltage divider consists of two resistors and is used to lower the voltage to a level that is appropriate for the MCU. Following the voltage divider, a filtering capacitor is used for EMC protection. Finally, a Zener diode is used for overvoltage protection.

Protecting the input pin of an MCU in automotive electronics is crucial as any damage or failure could lead to severe consequences. A well-designed protection circuit provides a reliable and robust solution to protect against various threats, such as electromagnetic interference, electrostatic discharge, and voltage spikes. By implementing a multi-stage protection circuit that includes an EMI/ESD capacitor, pull-up resistor, voltage divider, filtering capacitor, and Zener diode, designers can ensure the longevity and reliability of their circuits, even in harsh environments.

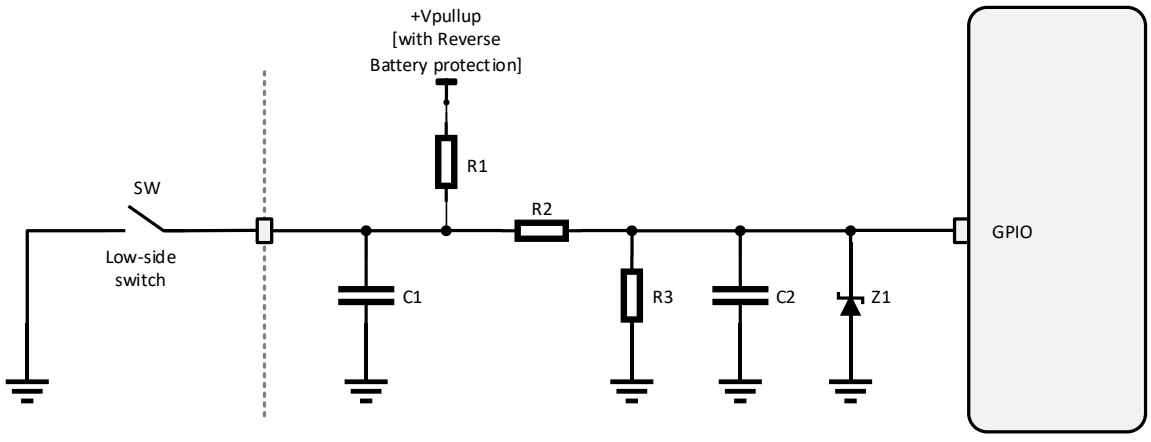


Figure 43. Input Circuit - Low-side switch circuit with passive resistors

Table 17. Component description for the Low-side switch circuit with passive resistors

Symbol	Description
C1	ESD protection and EMC filter
C2	EMC filter and low-pass filter in conjunction with R2‖R3 to filter input noise
R1	Primary load for the source switching device to provide wetting current for contacts and connectors. A low impedance also helps to reduce cross-talk
R2	Forms a voltage divider with R3. Limits current into the load and with R3, forms a low-pass filter with C2.
R3	Forms a voltage divider with R2
Z1	Zener diode to provide a protection against overvoltage The Zener diode should be selected based on upper limit of thee normal voltage operation. This ensures protection against overvoltage conditions.

14.1.4 Low Side Switch – Level Shifter with a NPN Common Emitter Transistor

This circuit serves the crucial function of interfacing a microcontroller (MCU) with an external Low-side switch, in other words, specifically a switch that connects to ground when closed. The primary component of this circuit is an NPN transistor (Q1), acts as a logical switch, ensuring safe voltage and current levels for the MCU's GPIO pin.

To protect the MCU against injection current and other potential issues, the circuit incorporates several elements. First, an input capacitor (C1) will provide an ESD protection and EMI filtering. Connected to this node is a pull-up resistor (R1) that ties the input to a positive voltage source with reverse battery protection. R1 ensures that Q1 remains in saturation mode and maintains a high logic level at the MCU's GPIO pin when the external low-side switch is open. Additionally, two resistors (R2 and R3) are linked to the base of Q1, forming a voltage divider. This divider restricts the base current to Q1, helping to control its operational mode effectively. The base of the NPN transistor also includes a capacitor (C2), which, together with R2 and R3, forms a low-pass filter. This filter assists in reducing noise and ensuring stable transistor switching. Finally, at the collector of Q1, a load resistor (R4) connects to the MCU's logic voltage level. This resistor acts as a current limiter, preventing excessive current from flowing into the GPIO pin.

In summary, this circuit provides a comprehensive solution to safely interface an external low-side switch with an MCU, ensuring reliable and protected operation.

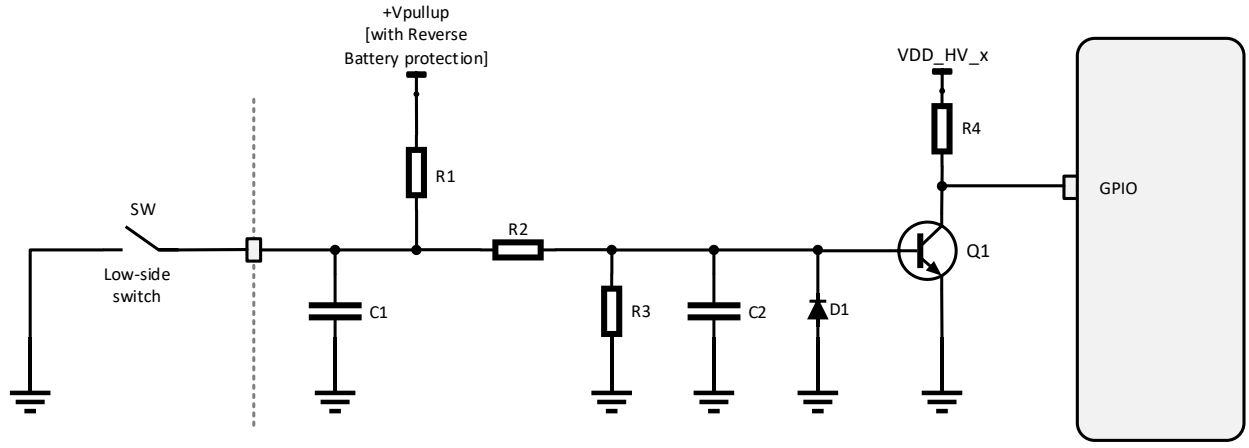


Figure 44. Input Circuit - Low-side switch circuit with a NPN Common Emitter Transistor

Table 18. Component description for the Low-side switch circuit with a NPN Common Emitter Transistor

Symbol	Description
C1	ESD protection and EMC filter
C2	EMC filter and low-pass filter in conjunction with R2‖R3 to filter input noise
R1	Primary load for the source switching device to provide wetting current for contacts and connectors. A low impedance also helps to reduce cross-talk
R2	Forms a voltage divider with R3. Limits current into the load and with R3, forms a low-pass filter with C2.
R3	Base-emitter bias resistor for Q1. Forms a voltage divider with R2. The resistor helps to keep the transistor off by shunting collector-base junction leakage current to ground.
D1	Reverse voltage protection for Q1's base-emitter junction.
Q1	Small-signal transistor to buffer the input and act as a digital switch.
R4	Load resistor for Q1.

14.1.5 Analog Voltage sense

Within the realm of automotive electronics, the development of an input conditioning circuit takes on paramount importance when dealing with a high-voltage analog signal that needs to interface with a microcontroller's ADC port. This circuit has a singular mission: the precise measurement of high-voltage at battery levels. The linchpin of this circuit is undoubtedly the voltage divider [R1 and R2]. This indispensable section has a dual purpose. Firstly, it scales down the high input voltage to a level that's compatible with the microcontroller's ADC. Secondly, it acts as a barrier, limiting the input current, and ensuring the microcontroller remains unscathed and within its operational limits.
The Zener diode plays a pivotal role in safeguarding the entire system. It's the first line of defense against voltage transients that may occur in the battery voltage, effectively clamping down on voltage spikes and protecting the microcontroller from potential damage. Last but not least, we have capacitor C2, working with resistors R2 and R3. Together, they constitute a low-pass filter. This filter is instrumental in removing high-frequency noise from the analog signal, ensuring that the microcontroller receives a clean and accurate representation of the battery voltage.

This circuit offers robust protection against two critical risks: "injection current," which poses a threat to the microcontroller, and "electrical over-stress" (EOS), which could undermine its long-term reliability of the MCU.

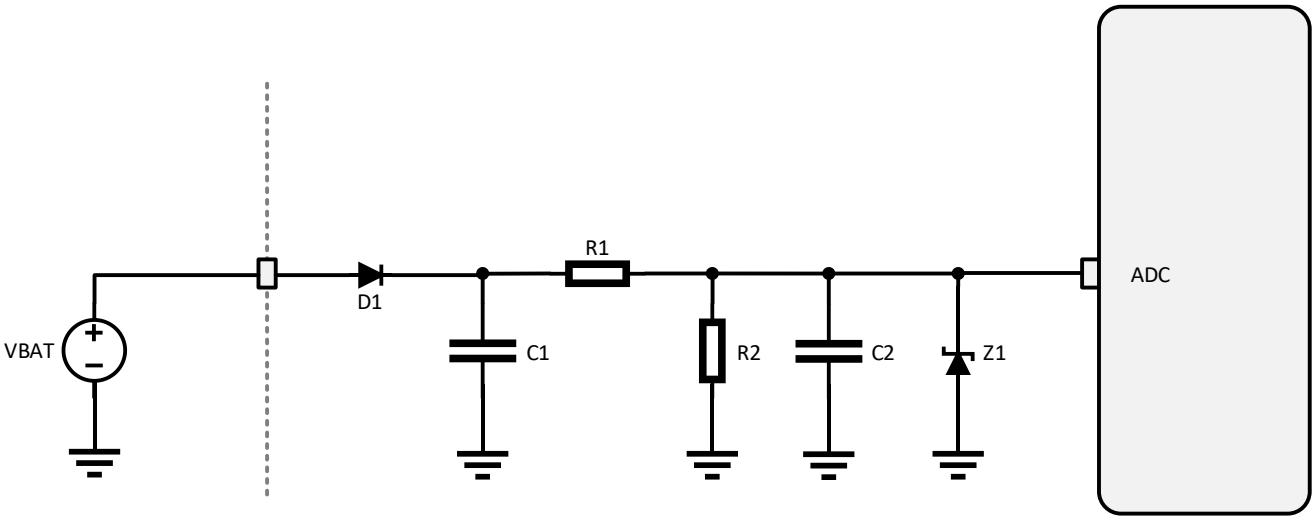


Figure 45. Input Circuit - Analog Voltage sense

Table 19. Component description for the Analog Voltage sense circuit

Symbol	Description
C1	ESD protection and EMC filter
C2	EMC filter and low-pass filter in conjunction with R1‖R2 to filter input noise. C2 also acts as a charge reservoir to maintain a constant voltage when the output is sampled by the ADC port.
R1	Forms a voltage divider with R2. Limits the current into the load and with R2 forms a low-pass filter with C2.
R2	Forms a voltage divider with R1
Z1	Zener diode to provide a protection against overvoltage The Zener diode should be selected based on upper limit of thee normal voltage operation. This ensures protection against overvoltage conditions.
D1	Reverse voltage protection

15 Package

The S32M2 MCU is offered in the following package types

Table 20. Packaging

Package Type	Document number
64LQFP_EP	98ASA10763D

16 References

- Crystal Oscillator Troubleshooting Guide - NXP Semiconductors
- AN2049 - Some Characteristics and Design Notes for Crystal Feedback ...
- AN10853 - ESD and EMC sensitivity of IC - NXP Semiconductors
- AN2321 - Designing for Board Level Electromagnetic Compatibility - NXP Semiconductors
- AN10897 - A guide to designing for ESD and EMC

17 Revision history

Table 21. Sample revision history

Revision number	Date	Substantive changes
1.0	10/2023	Initial release

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